Updated Results from Deep Trek High Temperature Electronics Development Programs

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Introduction

Electronics are used in modern oil and gas exploration to collect, log, and/or process data such as heading and inclination, weight on the bit, vibration, seismic/acoustic response, temperature, pressure, radiation, and resistivity of the strata. High-temperature electronics are needed that can reliably operate in deep-well conditions (up to 250°C). The U.S. Department of Energy Deep Trek program has funded two projects led by Honeywell. The first project, launched in 2003 and completed this year, established a production-level integrated circuit (IC) manufacturing process, components and design tools [1-4] specifically targeting high-temperature environments (up to 250°C). The second project, launched in 2006 and completing in 2008, will develop rugged packaging suitable for down-hole shock and vibration environments which will be used to house and demonstrate components developed in the earlier project. This paper describes updated results of these successful projects.

Deep Trek Projects

Oil and gas drilling time and costs escalate when the target reservoir is very deep. Relative to more conventional well depths it is therefore even more important to be able to monitor down-hole conditions in deep wells (>15,000ft, 4,575m). This creates a catch-22 situation because electronics that can reliably operate in deep-well conditions have not been available, primarily due to the high temperature (up to 250°C, 481°F) encountered at great depth. Commercial electronics are not designed for these temperatures, and conventional integrated circuit (IC) technology is not capable of operating at these temperatures. To help overcome this limitation, the U.S. Department of Energy Deep Trek program has funded two projects led by Honeywell to develop electronic components that can handle the heat and deliver the data operators need to undertake deep-reservoir development.

The first project, launched in 2003 and completed this year, established a production-level IC manufacturing process along with IC design tools (software and simulation elements) specifically targeting high-temperature environments. These IC technology and design tools were then employed to develop prototype high-temperature IC components, with the objective that these will be made available to the industry as commercial products. This project was completed in collaboration with a Joint Industrial Participation (JIP) consortium of commercial partners. The JIP partners defined priorities and specifications for components developed and demonstrated within the project. These include:

- a dual precision amplifier,
- a field programmable gate array (FPGA),
- a high-resolution A-to-D converter,
- a high-temperature non-volatile memory (EEPROM).

An additional outcome of this project is a family of metal mask programmable gate-arrays suitable for use up to 250°C.

The second project, launched in 2006 and scheduled for completion in 2008, will develop rugged multi-chip-module (MCM) packaging suitable for down-hole shock and vibration environments. An MCM package developed under this project will be used to house and demonstrate components developed in the earlier project.

High Temperature Wafer Process Technology

A partially depleted 0.8 micron SOI CMOS IC manufacturing process has been developed and established in factory production specifically for high-temperature applications [5]. The wafer process flow was adapted from a previously established SOI technology in use for aerospace products. This adapted technology has been successfully applied in the manufacture of all of the proto-type IC components within these Deep Trek projects. All of the devices in this process are suitable for long-term operation (5 years at 225°C) using 5V supplies. Besides the use of SOI structure, the primary feature of the wafer process to address high temperature includes the adjustment of transistor threshold voltages to minimize sub-threshold leakage. Up to four layers of aluminium interconnect are available. Inter-connect electro-migration reliability is established by characterization and adherence to design rules limiting the maximum current density in the conductors, either through de-rating of operating frequency (for digital applications) or through high temperature optimized interconnect layout (primarily power bus and/or DC output conductors). Analog elements (CrSiN thin-film resistors, MOS capacitors, and lateral PNP transistors) are available and supported.

Temperature-compensated biasing techniques for analog circuits are employed to maintain gain and bandwidth over an extremely wide temperature range. Design toolkits have been updated and applied for high temperature applications. These include development of SPICE models applicable from -55°C to 250°C.

Purely analog (or full-custom digital) blocks are implemented using traditional analog tools and processes, including schematic entry and SPICE based simulation methodologies. This is done using a Process Design Kit (PDK) which is an integrated collection of schematic capture symbols, models, layout rules, and other items to allow use of design software available from Cadence. Laser-trimming and high temperature wafer probing can be combined to adjust voltage reference temperature coefficients, or for tailoring other temperature-dependent circuit performance.

Now that the first Deep Trek project has been completed this wafer process, layout rules, SPICE models, and Cadence design and layout toolkit items may be accessed on a foundry basis.

High Temperature Digital Gate Arrays and Design Infrastructure

Digital functions are commonly defined at a behavioural level in the form of hardware description language (HDL) netlists. Once defined by this means they are commonly implemented in hardware by a process of synthesis into a gate-level structure which is then fabricated using gate-array IC platforms. A family of metal-mask programmable gate arrays suitable for manufacture in the 0.8 micron SOI process (described above) has been validated for high-temperature use. This gate-array family (HT2000) uses established HDL-based development tools and flows [6, 7]. The conventional Honeywell design tools and techniques have been extended for high-temperature application. This includes simulation timing models that are applicable at 250°C, and load-checking routines for adherence to rules appropriate to address high-temperature electro-migration concerns. The HT2000 family of high-temperature gate-arrays incorporates a family of die encompassing a ranging from 27,000 to 275,000 usable gates. For ASIC designs incorporating a mix of analog and digital blocks, sub-modules of analog and/or custom digital circuitry may be embedded inside the gate-array I/O ring. For example, this was the means for implementing one of the high-temperature A-to-D converters in this project.

Dual Precision Amplifier

A high-temperature dual precision amplifier has been developed and fully-verified at 225°C with additional testing up to 375°C [8]. The component die size is 2.3mm x 1.8mm. The amplifier is continuously auto-zeroed to achieve very low offset and low-frequency noise, making it suitable for low-frequency DC-coupled sensor-interface applications. The auto-zero function requires a clocking source. The chip can provide this clock autonomously via an on-chip oscillator, or there is the option of providing an off-chip clock. Using an off-chip clock can provide more optimal performance, especially for sampled-data systems where usage of an off-chip clock can allow synchronization with the sampling period. The dual precision amplifier also has a sleep-mode feature to conserve power when the amplifier is not in use. Previously reported data from prototype characterization is summarized in Table 1 below. Manufacturing test programs have been developed and test/assembly flows have been established for commercial sales in the form of 14-pin DIP packages or as deliverable die.

TABLE 1 : Dual Precision Amplifier Packaged Test Data (-55°C to 225°C) unless noted

Parameter	Target Value	Measured Results
Input Offset Voltage	±100 μV (max.)	±5 μV (external clock)
Supply Current (5.25V supply, 225°C)	5 mA	1.85 mA
Open-loop Gain (-55°C to 225°C)	> 100dB	> 114dB
Input Noise Voltage RS=100Ω, 0.1Hz – 10Hz (internal clock) (External clock at 30KHz)	 3 μV pk-pk	5.7 μV pk-pk @ 23°C 4.6 μV pk-pk @ 225°C 1.4 μV pk-pk @ 23°C
Input Range	V_{SS} to V_{DD} -2.0	V_{SS} to V_{DD} – 1.7
Output Source/Sink (swing to 0.3V from either rail)	±20 mA	> 20 mA
Output Short-Circuit Current Limit	±50 mA	51 mA (average)
Supply Current with Shutdown asserted	150 μA, maximum	13 uA, typical

High-temperature Field Programmable Gate Array

Low-volume digital IC applications are often addressed by the use of programmable logic devices. These go by a variety of names, including Field Programmable Gate Arrays (FPGAs). FPGAs apply the economic advantages of batch processing to low-volume or application-specific digital components by enabling the user to customize components on a unit-by-unit basis. An FPGA is configured by electrical means, such as writing to configuration memory (in the case of a reconfigurable FPGA) or else by a process of permanently configuring the part by electrical fusing.

FPGA products are not commercially available for the extreme high temperature environment (at or above 225°C) required by the Deep Trek program. Therefore, a high-temperature FPGA has been developed under the Deep Trek program. It is a licensed functional equivalent to a commercial FPGA, the Atmel AT6010 [9]. The high temperature FPGA has been designed using the HTSOI process for specified operation at 225°C. It is a re-programmable, SRAM-based FPGA that provides 30,000 programmable logic gates and 204 programmable inputs/outputs. Configuration is controlled by dedicated configuration pins and dual-function pins. Dual function pins double as user I/O pins after the device is configured and in operation [10]. The devices can be partially reconfigured while in operation; where portions of the device not being modified remain operational during reconfiguration. The high-temperature FPGA has been fully verified by wafer-probe testing at 200°C (391°F). The design includes more than 3 million transistors, yet standby leakage current at 200°C is still under 0.5mA. This design will be offered in die-form, as well as embedded within the RPDA multi-chip module described later.

High-temperature A-to-D Converters

Two complete high-temperature A-to-D converters have been proto-typed. The first, a high-resolution A-to-D was funded under the Deep Trek program [4]. The second, a 12-bit successive-approximation A-to-D was completed in parallel with the Deep Trek program. A comparison of features and performance is provided in Table 2.

The Deep Trek A-to-D was developed to digitize DC and very-low frequency signals to a high level of resolution. The design provides 20-bits of resolution, although effective performance was not expected beyond 18-bits. The Deep Trek program intent is to develop a high-resolution A-to-D (targeting 18-bit performance) suitable for industry use as a commercial product (referred to as HTADC18). A block diagram of the HTADC18 is shown in Figure 1. The core A-to-D function is provided by a 2^{nd}-order sigma-delta modulator with a single-bit output at an over-sampling ratio of 2048 (single-bit modulator output rate is 204.8KHz). An on-chip digital decimation and filter processes the modulator output to develop a 20-bit conversion result at 100 samples per second. Other features include a Reference and PTAT (Proportional-To-Absolute Temperature) block [11]. This block generates voltage-reference and current-reference outputs, as well as a PTAT current source, and a "thermometer" voltage. The thermometer voltage was designed for use as an on-chip temperature monitor. The HTADC18 also includes an auxiliary 8-bit successive approximation A-to-D which can be used to digitize either this temperature signal or an external signal source depending on the user's preference. The HTADC18 incorporates a self-contained oscillator so that the A-to-D can function autonomously, and a serial I/O block (Serial Peripheral Interface, or SPI). Using the SPI the HTADC18 can be configured to operate in several modes, or be placed into sleep state to minimize power consumption when not in use. Also via the SPI the HTADC18 can be configured so that the raw modulator output and 204.8KHz sampling clock are available on the

MDO and CLKOUT pins respectively. This last feature enables potential use with external decimation and filtering functions that might be employed to achieve faster update rates at the price of overall resolution.

TABLE 2 : High-temperature A-to-D Converter Features and Prototype Performance

Feature	Deep Trek High-Resolution A-to-D	12-bit A-to-D
Output Resolution	20 bits	12 bits
Architecture	2nd order sigma-delta	Successive Approximation
Update Rate	100 Samples/sec	100K Samples/sec
Input	Differential (with single-ended option)	Single-ended
Output format	Serial	Parallel
DC Linearity at 225°C	16.7 bits	10.7 bits
Power Dissipation at 225°C	35mW	
ENOB at 225°C	17.4 bits	
Output repeatability	17.7 bits (RMS), 15 bits pk-to-pk	
Die Size	10.4 mm x 9.5 mm	3.2 mm x 2.8mm
Prototype Package Configuration	28-pin DIP	28-pin DIP

The HTADC18 was implemented by partitioning the design between analog functions (oscillator, modulator, 8-bit ADC, Reference and PTAT block) and digital functions (digital filter and serial data interface). Analog functions were collected into a single analog/mixed-signal block and dropped into a high-temperature gate-array die which contains all digital functions. Digital blocks are synthesized from behavioural HDL using the high-temperature HT2000 toolkit and design platform.

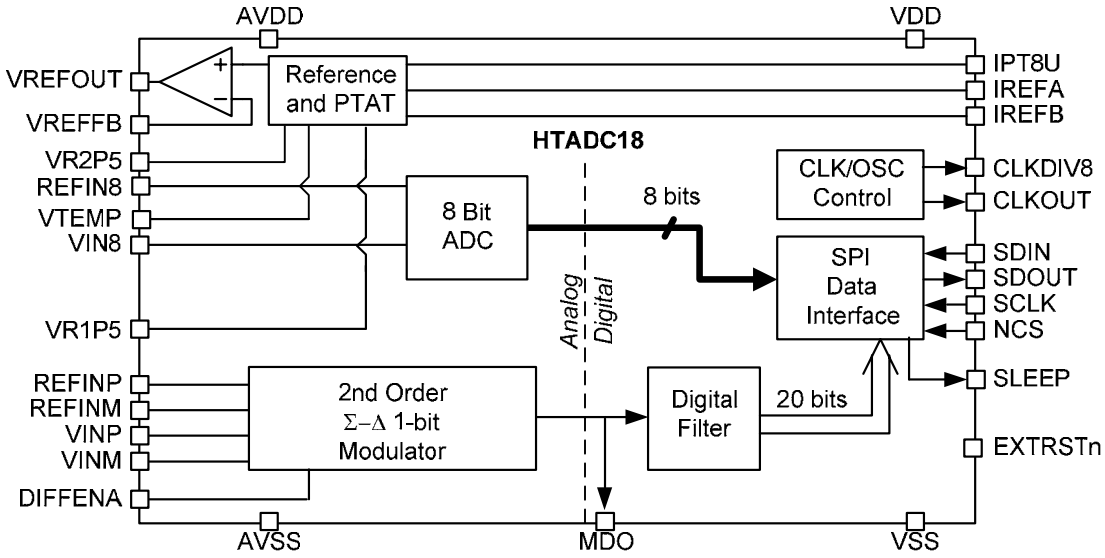


FIGURE 1: Deep Trek High-Resolution A-to-D (HTADC18) Block Diagram

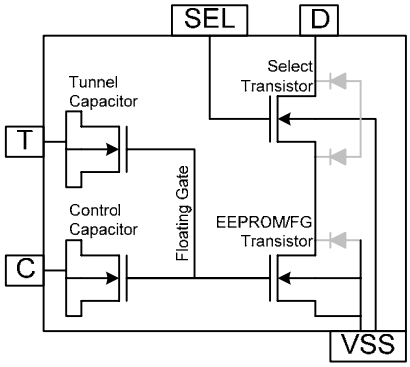
Two design iterations of the HTADC18 have been completed. After a final assembly process flow is developed the HTADC18 will be capable for commercial sale in a 28-pin DIP package.

The 12-bit A-to-D converter is a successive approximation A-to-D based using an embedded capacitive charge re-distribution DAC. This recently fabricated design is an extension to 12-bit resolution of the auxiliary 8-bit ADC that is embedded within the Deep Trek HTADC18. Prototype evaluation over temperature shows a repetitive non-linearity that occurs with every 64 output codes. This is most likely caused by a systematic matching error in the capacitor array of the DAC. Including this error, overall linearity is within plus/minus 2.5 LSB's. This should be easily improved to plus/minus 1.5 LSB's assuming that the systematic DAC error can be identified and eliminated.

High-temperature EEPROM

A high-temperature non-volatile memory was one of the chief component objectives of the Deep Trek High-Temperature Electronics program. The resulting high-temperature EEPROM (HTEEPROM) development was logistically constrained to an approach that could be implemented in the Deep Trek HTSOI wafer process flow with no additional processing steps. For this reason a single-poly floating gate structure was chosen as the basis for a non-volatile memory cell.

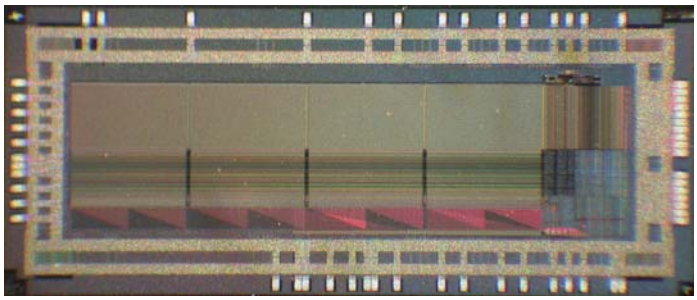
During the course of the program three cycles of design and fabrication have been completed. The first was focused on development and characterization of single-poly floating-gate memory cells (see Figure 2). EEPROM operation is based upon shifting the threshold voltage of floating-gate transistors by adding or removing charge by Fowler-Nordheim tunnelling. The threshold shift is read by turning on the floating gate device by capacitive coupling and detecting the difference in current resulting from a positively versus negatively shifted transistor threshold. Memory cell structures selected for further development were tested for data retention at 250°C for over 11,000 hours.



- **Charge is added or removed from the floating gate by Fowler-Nordheim tunneling through the tunneling capacitor oxide (voltage applied to terminals "T" and "C"**
- **Net effect is an apparent threshold voltage shift in the EEPROM transistor**
- **Memory cell is read by turning on the EEPROM transistor by capacitive coupling using the Control Capacitor**
- **Drain current is sensed to detect the difference between a "programmed" cell (stored 1) and an "erased" cell (stored 0)**

FIGURE 2: Single-poly Floating Gate Memory Cell

After the first round of silicon (focused on memory cell development), a second round of silicon was dedicated to a test-chip that focussed on arraying cells into a typical product configuration and validating means for accessing individual cells within the array for reading and writing. The demonstration vehicle was a 32Kbit memory array accessible as a 4K by 8 bit memory. This incorporated high-voltage row/column interface circuitry required for memory cell writing. High-voltage generation and waveform shaping for memory cell program/erase were generated off-chip. This demonstration memory (Figure 3) was used to verify capability for reading and writing over the full temperature range as well as further testing of data retention and data cycling in the array.



- **Off-chip program/erase waveform generation**
- **Demonstrated read/write at 250°C**
- **Data retention testing >500hrs @250°C**
- **Memory array program/erase to 100K cycles**

FIGURE 3: 32Kbit Demonstration Memory Array

Based on results from these first two test chips, a 32K x 8 HTEEPROM product design has been designed and fabricated. By means of a configuration input pin, this memory can be configured for either parallel or serial interface. The parallel interface incorporates the functionality of industry standard 28C256 parallel memories (see Figure 4). In addition it adds six I/O that are dedicated for use with the High-Temperature FPGA (these are identified by the blue font in the table embedded in Figure 4). These I/O enable the HTEEPROM to serve as a non-volatile programming device (i.e., configuration memory) for the High Temperature FPGA, capable of autonomously configuring the FPGA on power-up. The HTEEPROM also adds pins for connection to external capacitors that are required for the charge pumps that generate the high-voltage (plus/minus 8.25V) supplies needed to write the HTEEPROM.

Pin Name	Description
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
FPOR	**FPGA Power On Reset**
CCLK	**Configuration Clock**
ERR	**Configuration error flag**
CON	**Configuration Handshake**
DEFCON	**Enable FPGA SRAM Check**
CHECK	**Start SRAM Check Cycle**
A0-A14	Address Inputs
D0-D7	Data Inputs/Outputs

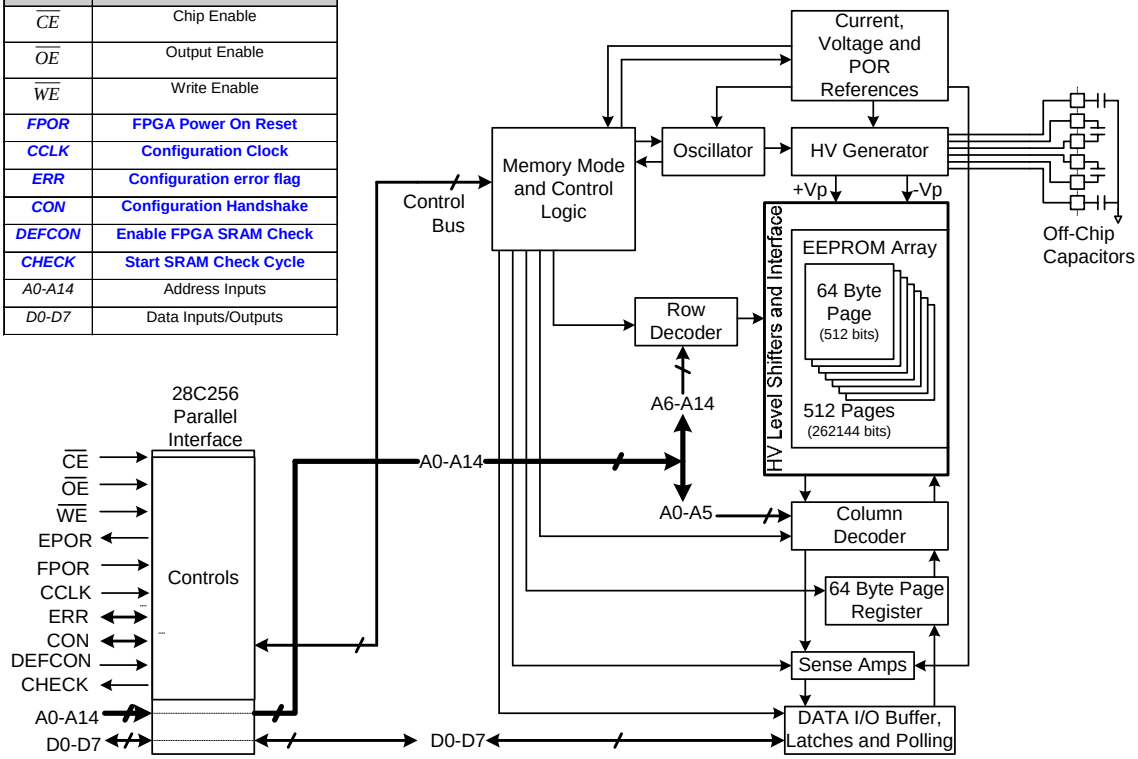
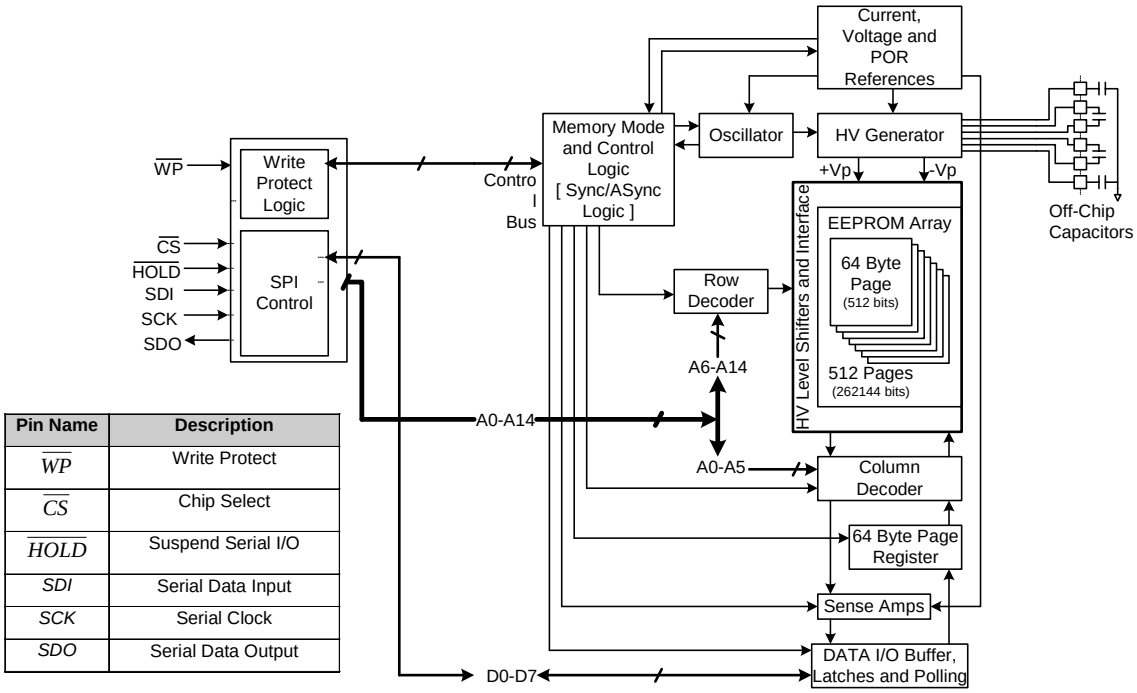


FIGURE 4: HTEEPROM Parallel Interface Configuration
(Signals listed in blue font are used for High-temperature FPGA configuration)

The serial interface configuration is shown in Figure 5. Comparison to figure 4 shows that the core functionality is not changed between the two approaches. A small amount of logic is added to the core to implement the serial interfaced control shown in Figure 5. The serial configuration incorporates the functionality of industry standard 25C256 memory devices.



Pin Name	Description
$\overline{WP}$	Write Protect
$\overline{CS}$	Chip Select
$\overline{HOLD}$	Suspend Serial I/O
SDI	Serial Data Input
SCK	Serial Clock
SDO	Serial Data Output

FIGURE 5: HTEEPROM Serial Interface Configuration

The complete 32K x 8 HTEEPROM product design has recently completed fabrication. Design verification testing will be completed during the second half of 2007. It is expected that this design will be commercialized in the form of deliverable die as well as in packages. Package development has yet to be completed.

High-temperature Multi-chip Module / RPDA Project

Honeywell was awarded a second Deep Trek project in 2006 that focuses on packaging aspects of high-temperature electronics. This new project is entitled Re-configurable Processor for Data Acquisition (or RPDA). The objective is to develop a rugged co-fired ceramic multi-chip module suitable for down-hole oil and gas exploration and/or down-hole permanent installation applications. The RDPA package will house the Deep Trek High-temperature FPGA, the HTEEPROM, and a previously developed high-temperature SOI 32K by 8 bit SRAM (HT6256). The floor-plan of the top-view looking into the RPDA package is shown in Figure 6. The underside of this package is populated with 147 pins arranged as a 7 by 21 grid on 0.1 inch spacing. In addition to the FPGA, EEPROM and SRAM, the package also will house ceramic chip capacitors required for the EEPROM charge pumps as well as power-supply transient by-pass capacitors. These capacitors, as well as all other components and materials will be capable for use at 225°C or higher.

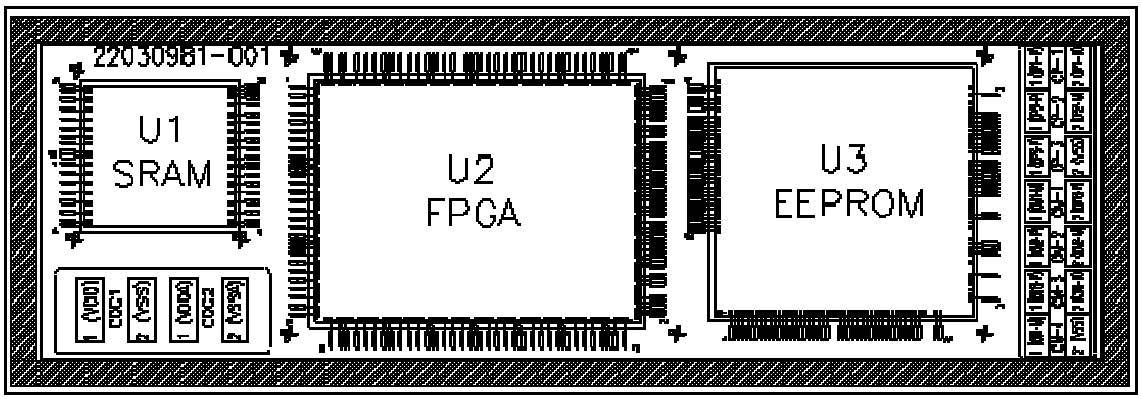


FIGURE 6: RPDA Package Component Floorplan, Top View.
Overall dimensions are 5.558 cm by 1.905cm

The RPDA package will have multiple layers of embedded interconnect. The inter-connect and I/O assignment are designed so that comprehensive testing of the individual IC's can be performed after all components have been assembled in the package. The FPGA and EEPROM interconnect will facilitate configuration of the FPGA by multiple modes, including autonomous configuration of the FPGA using data that can be pre-loaded into the EEPROM. The package will provide 55 fully configurable I/O which the user can define according to the FPGA configuration. An additional 57 I/O will have direct access to the SRAM and/or EEPROM, but can also be configured by the user. At this writing the MCM package is in the final design phase, and fabrication is planned for completion in early 2008.

In addition to the package development, the RPDA program also is chartered to develop and demonstrate configuration of the RPDA for a data acquisition function. At this time the planned configuration targets using the RPDA module to control and capture data from an external HTADC18 A-to-D converter under sampling schedules that may be established remotely via a master SPI control device. By the completion of the program in the first half of 2008 the RPDA package will be developed, fully assembled, and demonstrated in both an un-configured state as well as configured for the targeted data acquisition functional demonstration.

Summary

U.S. government and industry collaborative research under the Deep Trek programs have resulted in the successful development of SOI technology and design infrastructure for applications up to 250°C, including a family of high-

temperature mask-programmable gate arrays. These have been utilized for the development, prototyping, and high-temperature functional and parametric validation of multiple components. These components, important for the realization of practical down-hole electronic systems, include high temperature versions of a dual precision amplifier, two complete A-to-D converters, and a field-programmable gate array. In addition, technical feasibility has been established for high-temperature non-volatile memory in the HTSOI process, and this has resulted in the design and fabrication of a complete 32K by 8 HTEEPROM that is currently in design verification. Additional development under the Deep Trek program will result in a rugged package suitable for down-hole applications to house multiple components in order to develop a flexible Reconfigurable Processor for Data Acquisition (RPDA). All of these items, including design tools, wafer foundry access, and components are planned to be accessible by commercial channels within six to twelve months.

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