Technology and Tool Kit Development for the U.S. Department of Energy Deep Trek Program

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Introduction

This paper is an update of the high-temperature SOI electronics processes and toolkits that are being developed and utilized under the U.S. Department of Energy (DOE) Deep Trek High-Temperature Electronics program [1]. This program began in late 2003 and is expected to be complete by early 2007. The motivation for the Deep Trek program is to support technology development that makes deep oil and gas drilling economically viable. Down hole data acquisition systems are necessary to make deep drilling and reservoir production cost-effective. High temperature encountered at great depth (>200°C) is the single biggest obstacle for electronic data acquisition systems in very deep wells. Electronics needed in these environments include signal conditioning, A-to-D conversion, digital processing and control electronics, and memory (including non-volatile memory).

Commercial electronics are not designed for these temperatures, and conventional silicon integrated circuit technology is not capable of operating at these temperatures. It is well known that SOI CMOS is a viable alternative to bulk CMOS technology for high temperature [2]. However, most commercial SOI processes are optimized for consumer digital applications (i.e., optimized digital speed/power trade-off). These processes tend to be limited in terms of supply voltage, making analog and mixed-signal applications difficult. In addition, although junction leakage is reduced by SOI, sub-threshold leakage in low-voltage SOI processes may render them unusable for extreme high temperature because of unacceptably high standby current.

Therefore, some tailoring of the process for extreme temperature applications is needed, first to provide capability for analog as well as digital applications, and secondly to deal with sub-threshold leakage in very large digital circuits (memory, microprocessors, etc.). While the need for deep well instrumentation is compelling, and the ability to tap deep oil and gas is clearly in the public interest, electronic component manufacturers have not stepped up to meet this need because of the small market size relative to the investment required. The number of SOI foundries that specifically support high-temperature design (with wafer processes, models, high-temperature qualification, etc.) is very small. This is a major reason for U.S. DOE of support the Deep Trek program.

The specific objectives of the Deep Trek program include development and commercialization of a first set of high-temperature components to be used for down-hole data acquisition and control. These include a precision amplifier, a field-programmable gate array (FPGA), a high-resolution A-to-D converter, and non-volatile memory. To enable this development the Deep Trek program funding also supports the wafer process and design infrastructure which are the topics of this report.

The Deep Trek program uses a High-Temperature SOI (HTSOI) process developed with relatively minor changes to an SOI production-level process developed for high-reliability aerospace applications. In fact, this approach has been in use for some time, and is well established in terms of high-temperature capability [3, 4]. However, while the "baseline" aerospace process has been continuously maintained at production status as equipment and facilities have changed (including transition from 4" to 6" wafers), the HTSOI derivative process had become "out of date". Thanks to the Deep Trek program the HTSOI process has been updated and re-established at production status. In addition, the Deep Trek program funds have enabled qualification of process/device features to support high temperature analog

applications, including on-chip thin-film resistors, capacitors, and lateral bipolar transistors (for voltage reference application). The result is a commercial IC process that is capable both for large-scale digital and precision analog applications operating reliably at 225°C and above [5]. Deep Trek is continuing to fund device research and development to support high-voltage devices and floating-gate memory cells that are needed for high-temperature non-volatile memory.

It is not sufficient just to be able to fabricate high temperature silicon wafers. Front-end design processes and back-end assembly, test, and screening processes must also be supported. Required design support includes the ability to simulate performance over the full operating temperature. The Deep Trek program has developed SPICE models suitable for use up to 250°C. Digital ASIC cell libraries have been characterized for high temperature as well. Design processes are thus developed that support both full-custom analog flows and Hardware-Description-Language (HDL) based digital design flows. These are being employed under the Deep Trek program in the development of mixed analog/digital standard product designs. Standardized wafer test, assembly, and burn-in capability complete the mixed-signal ASIC capability.

High Temp. Wafer Process

Features of the mixed analog/digital process are shown in Table 1. NMOS and PMOS drain current vs. gate voltage curves are shown in Figure 1. These show the "leakage floor" (see the y-intercept of the curves) which increases by 3-orders of magnitude from 25°C to 250°C. It can also be seen that threshold voltage decreases at high temperature (curves shift left) and that the sub-threshold slope decreases. In most commercial SOI processes all of these effects would combine to contribute to "off-state" leakage. In the HTSOI process the threshold voltage is increased relative to the conventional temperature range process. This enables HTSOI to support high-gate-count digital circuits at high temperatures. With this threshold voltage adjustment it can be seen that leakage at high temperature is dominated purely by junction leakage up to 250°C and not increased by sub-threshold conduction.

For analog circuits two types of resistors are available within the process flow. Resistors made of poly-silicon deposited on field oxide have a target sheet resistance of 90 ohms per square (at 25°C). A thin-film CrSiN resistor option is also available with a sheet resistance of 2500 ohms per square (at 25°C).

An optional linear capacitor implant is also available within the process flow (see Figure 2). This results in an MOS capacitor structure where the capacitor bottom-plate is a heavily-doped N-type implant. The capacitor dielectric is formed by the same process sequence that forms the gate-dielectric for standard devices, and the top-plate is formed from gate poly-silicon. Measured capacitance typically is 0.6% lower at 250°C than at 25°C. Measured capacitance variation with voltage is less than 0.03% over ±5V range.

Table 1 : HTSOI Process Features

Process Feature	Typical Characteristics
Gate Oxide thickness	150 angstroms
Minimum transistor length	0.8 microns
Maximum Gate Oxide Voltage	5v
Target Vtn/Vtp 25°C 250°C	1.2V / -1.3V 0.85V / - 1.0V
Sub-Vt slope (mV/dec) 25°C 250°C	NMOS PMOS 150 180 260 320
Transistor "Off current" Nch, 250°C Pch, 250°C	 0.8 nA/micron width 0.5 nA/micron width
# of metal layers	3 or 4
Top Silicon Thickness	0.2 microns
Buried Oxide Thickness	0.4 microns
Partially/Fully depleted	Partially depleted
Poly-silicon resistors	90 ohms per square, 415 ppm/°C
CrSiN resistors	2.5K ohms per square, ± 300 ppm/°C
Linear Capacitor	670 angstroms, <150 ppm/Volt
Laser trim fuse links	Yes
Lateral PNP VREF	For delta-Vbe voltage reference generator only.

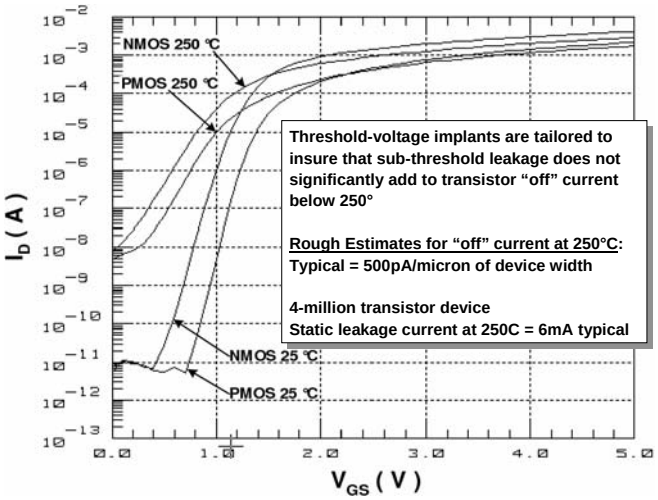

Figure 1: Log ID vs. Vgs for a 10/0.8 micron device at VDS=5V

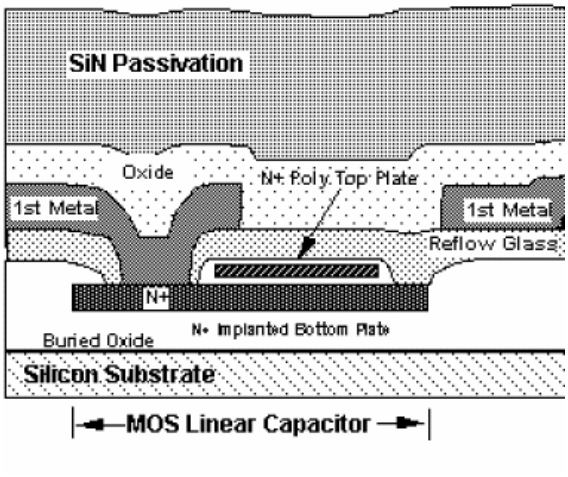

Figure 2: Capacitor Structure

One of the components to be developed under the Deep Trek program is a non-volatile memory. This will be based on data storage using a floating-gate device structure. To generate the tunnelling current to program/erase the memory bits will require the generation and switching of voltage on-chip that are on the order of 12V to 15V. This is beyond the capability of the standard transistors. This limitation may be overcome by layout techniques that emulate "lateral DMOS" approaches. The idea is to pull the N+ drain region away from the conducting channel and to extend the drain to the channel using the N-well implant (see Figure 3). This is done to minimize the maximum electric field applied across the gate oxide at the drain end of the device.

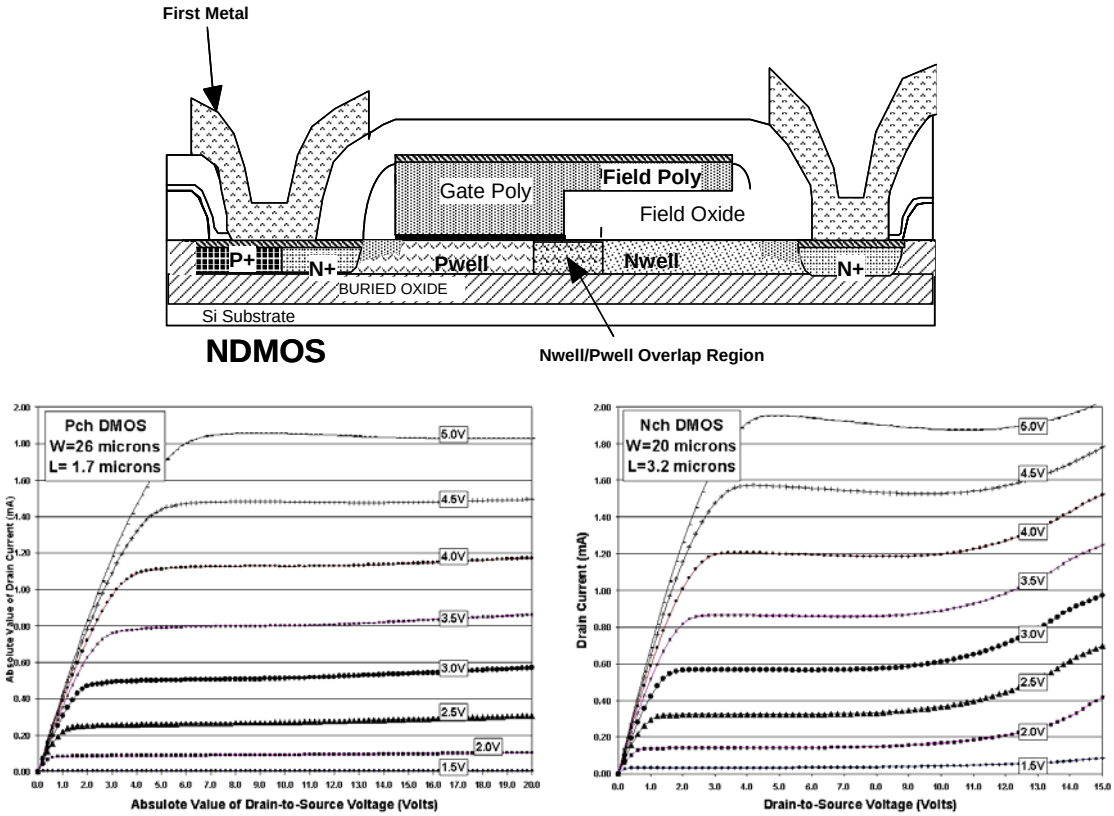

Figure 3: Extended Drain (DMOS) I-V Characteristics

I-V curves (at room temperature) are shown for an N-channel and P-channel devices in Figure 3. The I-V characteristics of these devices are strongly dependent on layout geometry. For the non-volatile memory application DMOS devices at much narrower widths will be required relative to the devices shown in Figure 3. Work is in

progress to characterize and model DMOS devices of various geometries in order to optimize the layout for the non-volatile memory application.

Lateral bipolar transistors can be fabricated in a partially depleted SOI process by re-arranging the terminals of the MOSFET so that source becomes emitter, drain becomes collector, and body-contact (i.e., Nwell/Pwell) becomes the base terminal. In this case the gate should be connected so that it does not affect device operation (most conveniently accomplished by connecting gate to emitter). Lateral transistors made this way suffer from very high base resistance and are therefore typically limited to very low frequency and/or low-current applications. For this reason it is not expected that lateral bipolar transistors will be used except within band-gap reference circuits. They can also be used to generate bias current and/or voltage sources with PTAT (Proportional To Absolute Temperature) characteristics. Characteristics for a bandgap reference circuit are shown in Figure 4.

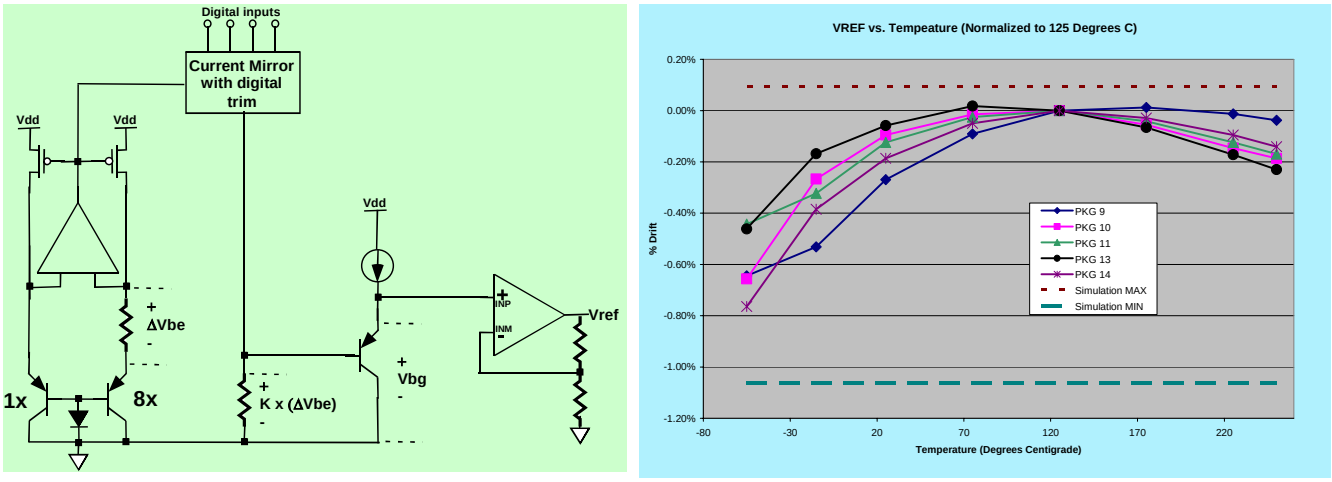

Figure 4 : Bandgap Voltage Reference Using Lateral PNP Transistors

Wafer Process Development Summary

Under the Deep Trek electronics program the HTSOI process has been fully re-characterized at the device level. This included running multiple wafer-lots containing device-level characterization structures so that statistical process variation is established and used to form criteria for wafer-lot acceptance as well as simulation. This update was necessary since many equipment and process flow changes had taken place since the initial high-temperature process work was completed for digital applications only. These process flow changes, including the conversion from 4-inch wafers to 6-inch manufacturing, made it risky to use existing SPICE models and digital timing parameters. The process changes also included the addition of 4th layer metal, and incorporation of analog process enhancements already discussed. As a result the HTSOI wafer process has been fully upgraded to production status.

ASIC Design Infrastructure Features and Flow

The HTSOI wafer process used by the Deep Trek program is layout-rule and photo-mask compatible with Honeywell's military temperature range aerospace technology. This has made it possible to leverage previously developed gate array platforms and design processes for digital ASICs and to provide Deep Trek program participants with a complete high-temp ASIC design platform [6]. This existing SOI ASIC infrastructure includes fully supported pad frames, under-layers, probe cards and packages that are available for the high-temp community to support new analog, digital and mixed signal chip ASIC designs. These allow high-temp devices having the features outlined in Table 2 to be designed and fabricated.

Honeywell's HTSOI ASIC design flow can be used to develop ASICs having almost any combination of analog and digital blocks. These capabilities range from full-custom analog to mixed analog and digital to completely digital ASICs. Analog designers have access to a library of SPICE primitives as well as a small library of digital cell primitives to use when implementing their designs. For digital designs, Honeywell's HTSOI4 digital cell library has been fully characterized for operation over the -55°C to +250°C temperature range. For the Deep Trek program, the "nominal" operating condition has been assumed to be +175°C and timing models are specifically developed to represent this typical condition as well as the other temperature extremes. Standard digital flows provide support for

many industry standard digital tools. Full custom analog and digital blocks can be dropped into the gate array and verified by simulation and layout verification tools. The gate array toolkit has been tailored to incorporate multiple power-supply domains, allowing for separation of analog vs. digital supplies. This includes separation of ESD protection networks which are otherwise a means for supply coupled crosstalk between analog and digital domains. The design libraries, tools and flows were proven out during the implementation of a mixed signal Sigma-Delta A-to-D converter developed by the Deep Trek program.

Table 2: High-Temperature ASIC Features

Product	Total Gates	Maximum Packaged Signal I/O	Max Available Signal I/O	Usable Gates 3 Metal Layers	Usable Gates 4 Metal Layers
HT2080	84,512	172	176	52,000	72,000
HT2160	159,528	240	240	91,000	126,000
HT2300	295,392	320	336	156,000	216,000
HT2400	389,120	320	338	200,000	275,000

Different design flows are used in the implementation of a high-temp ASIC; one design path for the analog block and a separate path for the digital block. Purely analog (or full-custom digital) blocks are implemented using traditional analog tools and processes, including schematic entry and SPICE based simulation methodologies. This is done using a Process Design Kit (PDK) which is an integrated collection of schematic capture symbols, models, layout rules, and other items to allow use of design software available from Cadence. Cadence Virtuoso® Schematic Editor is used for schematic entry. Cadence Spectre® and Ultrasim® are used for analog core simulation. Cadence tools are also used for analog core layout, parasitic extraction, merging analog and digital layout databases and for layout verification.

Meanwhile, purely digital blocks use conventional digital HDL-based development tools and flows. Conventional Honeywell HT2000 ASIC design tools and techniques are used to implement the high-temp ASIC. Digital functions are translated from functional RTL (Register-transfer-level) HDL code into structural gate-level netlists, typically using Synopsys Design Compiler® software. Many HDL simulation tools are available for functional and timing simulation of the synthesized blocks. These are placed and routed in the Gate-array core and loading and routing parasitics are extracted and annotated onto the netlists. Timing is verified using Synopsys Primetime® and timing models specifically developed for fidelity at high-temperatures.

For ASICs implementing a mix of analog and digital blocks, the two parallel and concurrent design paths will converge during mixed mode simulation of the entire chip and again during layout of the complete mixed signal ASIC. Designs are implemented in a hierarchical manner and, in order to simplify the simulation and back-end tool flows, the analog and digital sub-modules of mixed signal ASIC designs are segregated into separate sub-modules and instantiated into a single Verilog netlist module that implements the chip top-level interconnect. Interconnection of the analog and digital cores is verified by the Cadence AMS Designer simulator or other mixed mode simulation tool. Physical layouts of the analog and digital sections are merged to construct the final top-level chip layout.

The complete design can consist of a number of component blocks including an analog core, embedded custom SRAM, digital sub-blocks, I/O and top-level interconnect blocks. It may also include digital scan chain (inserted by software to enable Automated Test Pattern Generation, ATPG) and clock and reset multiplexing implemented using a mix of VHDL and Verilog languages. Note that VHDL RTL designs are converted to Verilog during logic synthesis to provide a consistent netlist for back-end tools and to allow for mixed mode simulation using cell primitives

In addition to supporting 3rd party software from a variety of CAE tool vendors, the design flow also incorporates proprietary software (i.e., specific to Honeywell's ASIC family) that check for loading violations, violations of electro-migration current density rules (limits are tailored specifically for high-temperature use), digital edge-rate violations, I/O placement errors, etc. The supported CAE tools help maintain highest design quality and help ensure an error free design.

Results: Sigma-delta A-to-D Converter Design Implementation

The design and process infrastructure developed for the Deep Trek High-Temperature Electronics Program have been used to develop a mixed-signal ASIC implementation of a high temperature sigma-delta A-to-D converter (Figure 5). This A-to-D includes the sigma-delta modulator, on-chip voltage reference, digital filters, and serial interface. It is implemented using the HT2160 gate-array with custom analog drop-in section and multiple power-supply domains. This design is currently in wafer fabrication and testing is expected to begin during fourth quarter of 2005.

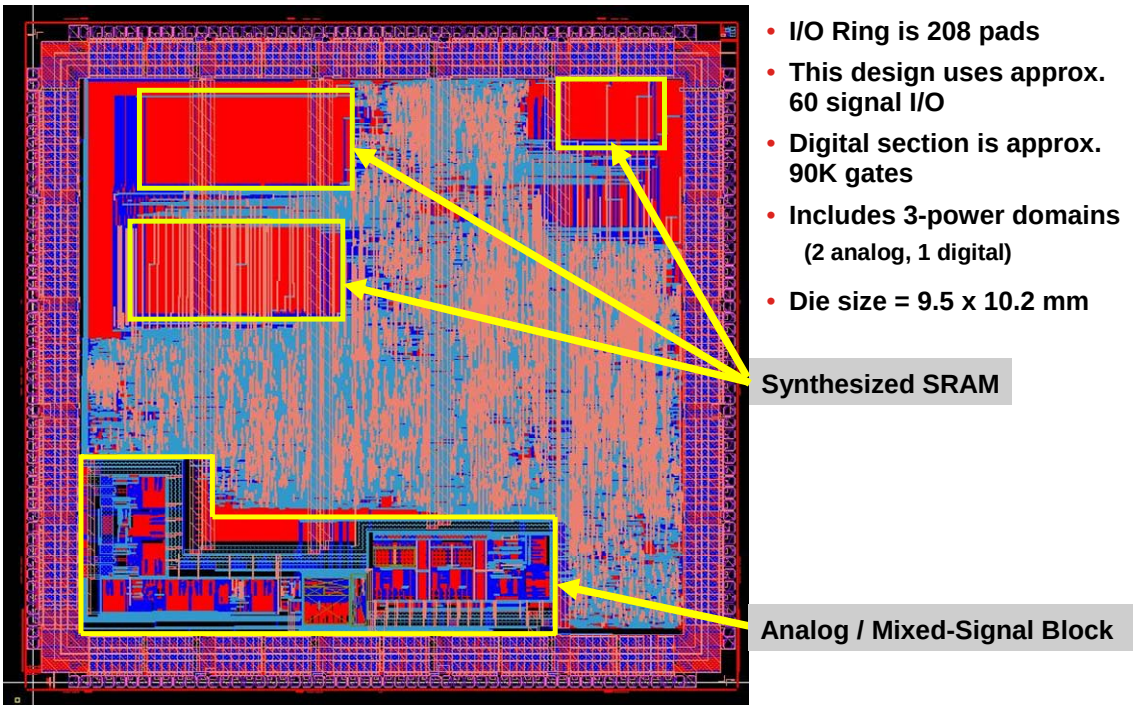

Figure 5: A-to-D Converter Layout

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