REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Vendor change for 2.5 V I/O capability in sections 1.3, 1.4, 3.2.9, and 6.9; table IA; Figures 2, 5, and 6. - llb	16-03-21	Charles F. Saffle

REV																				
SHEET																				
REV			A	A	A	A	A	A	A	A	A	A	A							
SHEET			15	16	17	18	19	20	21	22	23	24	25							
REV STATUS					REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS					SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Laura Leeper Branham	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Laura Leeper Branham	
	APPROVED BY Charles F. Saffle	MICROCIRCUIT, MEMORY, DIGITAL, CMOS/SOI, 16MBIT, RADIATION-HARDENED, NONVOLATILE RANDOM ACCESS MEMORY (NVRAM), MONOLITHIC SILICON
	DRAWING APPROVAL DATE 14-06-30	
AMSC N/A	REVISION LEVEL A	SIZE A · CAGE CODE **67268** · **5962-13212**
		SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	H	13212	01	V	X	C
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

_______________ _______________/
V
Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Temp Range	Configuration
01	HXNV01600	Rad-hard 16Mb Non-Volatile MRAM	-40 to +125°C	1/ 2/ 3/

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	76	Shielded ceramic quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Device type 01 is susceptible to magnetic fields.
2/ Device type 01 can be configured as either a 1048576 word x 16 bit device or a 2097152 word x 8 bit device.
3/ Device type 01, when provided as class Q, will have additional testing as defined in section 4.2.1.d.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range I/O (V_{DDIO})	-0.5 V dc to +4.6 V dc	
Supply voltage range Core (V_{DDD})	-0.5 V dc to +4.6 V dc	
DC input voltage range (V_{IN})	-0.5 V dc to V_{DDIO} + 0.5 V dc	
DC output voltage range (V_{OUT})	-0.5 V dc to V_{DDIO} + 0.5 V dc	
DC or average output current (I_{OUT})	90 mA	3/
Storage temperature	-65ºC to +150ºC	4/
Lead temperature (soldering 5 seconds)	+220ºC	5/
Thermal resistance, junction to case (θ_{JC})	4.0 ºC/W	
Output voltage applied to high Z-state	-0.5 V dc to V_{DDIO} + 0.5V dc	
Maximum power dissipation	1.25 W	6/
Case operating temperature range (T_C)	-40ºC to +125ºC	4/
Maximum junction temperature (T_J)	160ºC	
Magnetic Field Exposure (write)	65 Oersteds	7/
Magnetic Field Exposure (read, standby or unbiased)	100 Oersteds	7/
Data Retention (-40ºC to +105ºC)	15 years	
Endurance (-40ºC to +105ºC)	$1x10^{15}$ cycles	4/

1.4 Recommended operating conditions.

Supply voltage range 3.3V I/O (V_{DDIO})	3.0 V dc to 3.6 V dc	
Supply voltage range 2.5V I/O (V_{DDIO})	2.25 V dc to 2.75 V dc	
Supply voltage range Core (V_{DDD})	3.0 V dc to 3.6 V dc	
Supply voltage reference (V_{SS})	0.0 V dc	
High level input voltage range (V_{IH})	0.7 x V_{DDIO} to V_{DDIO} + 0.3 V dc	
Low level input voltage range (V_{IL})	-0.3 V dc to 0.3 x V_{DDIO}	
Voltage on any pin (V_{IN})	-0.3 V dc to V_{DDIO} + 0.3 V dc	
Case operating temperature range (T_C)	-40ºC to +125ºC	4/
Storage temperature range (T_{STORE})	-40ºC to +150ºC	4/

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, method 5012) .... 99.99 percent

1.6 Radiation features 8/

Maximum total ionizing dose available (dose rate = 50 – 300 rad(Si)/s)	1×10^6 rad(Si)	
Single event phenomenon (SEP):		
No single event latch-up (SEL) occurs at effective LET (see 4.4.4.4)	≤ 120 MeV-cm^2/mg	
Heavy ion single event upset error rate (SER)	1×10^{-10} upsets/bit-day	9/
Proton Single event upset error rate (SER)	$1 x10^{-11}$ upsets/bit-day	9/
Neutron irradiation (1MeV equivalent)	$1 x10^{14}$ neutrons/cm^2	10/
Dose rate data induced upset (dose rate duration ≤ 20ns)	$1 x10^{10}$ rad(Si)/s	
Dose rate survivability (dose rate duration ≤ 20ns)	$1 x10^{12}$ rad(Si)/s	
Latch-up	Immune by SOI technology	

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltages are referenced to V_{SS}.

3/ Time at Absolute Rating shall not exceed one second.

4/ See section 3.2.10.

5/ Maximum soldering temperature can be maintained for no more than 180 seconds over the lifetime of the part. Resistance to Soldering Heat is compliant with MIL-STD-883, method 2036, Table 2036-1 Test Conditions B, H and I.

6/ Operating power dissipation plus output driver power dissipation due to external load must not exceed this specification.

7/ Limits shown are guaranteed at T_C = +25°C ±5°C.

8/ For details on RHA parameters and test results, contact the vendor.

9/ Projected performance based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100 mil Aluminum shield using Weibull parameters based on an analysis of test data and simulation results. Weibull parameters and other relevant attributes are available from the vendor upon request to calculate projected SER performance for other orbits and environments.

10/ Guaranteed but not tested.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Output load circuit. The output load circuit for functional tests shall be as specified on figure 5.

3.2.6 Timing characteristics and waveforms. The AC timing characteristics and waveforms shall be as specified on Figures 5 and 6, and applies to capacitance, read cycle, and write cycle measurements unless otherwise specified.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.8 Functional tests. Various functional tests used to test this device are contained in Appendix A (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.8.1 Voltage Regulator tests. This microcircuit contains an onboard voltage regulator necessary for proper operation of the device. The voltage regulator is enabled by default and cannot be disabled by the user. All testing specified by this drawing is performed with the voltage regulator enabled. Voltage regulator disabled testing performed by the manufacturer shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request.

3.2.8.2 Error Correction Circuitry (ECC) tests. This microcircuit contains onboard error detection and correction circuitry necessary for proper operation of the device. The ECC is enabled by default and cannot be disabled by the user. All testing specified by this drawing is performed with ECC enabled. ECC disabled testing performed by the manufacturer shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request.

3.2.8.3 Non-Volatility tests. This memory microcircuit retains data in the absence of applied power. Non-volatility testing performed by the manufacturer shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request

3.2.9 Power-Up/Down Sequence. The power-up/down sequence shall be as shown in figure 6. The MRAM is protected from write operations whenever V_{DDD} is less than V_{DDDWI} which was designed for approximately 2.65V and whenever V_{DDIO} is less than V_{DDIOWI} which was designed for approximately 1.90V. As soon as V_{DDD} is equal to or exceeds V_{DDD}(min) and V_{DDIO} is equal to or exceeds V_{DDIO}(min), there is a startup time of 2 ms before read and write operations can start. This time allows memory power supplies to stabilize. The CLK and WE pins need to be held low (V_{IL} or lower) until after the 2 ms startup is complete. During power loss or brownout where V_{DDD} goes below V_{DDDWI} or V_{DDIO} goes below V_{DDIOWI}, writes are protected and a startup time must be observed when V_{DDD} returns equal to or greater than V_{DDD}(min) and when V_{DDIO} returns equal to or greater than V_{DDIO}(min). Ramp rates on the V_{DDD} and V_{DDIO} supply should not exceed 1 second in duration for either rising or falling.

3.2.10 Operating and Storage Life. Operating and storage life is up to 15 years for case temperatures up to 105ºC; and up to 2 years for temperatures above 105ºC up to 125ºC. In addition, storage life is up to 504 hours for temperatures above 125ºC up to 150ºC. Within these bounds, performance requirements will be met. For applications outside these bounds, or for additional Magnetic Tunnel Junction (MTJ) operating and storage time information, contact the manufacturer.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Read/Write cycle Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the temperature range listed in section 1.3 herein. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.9 Data Retention (device powered or unpowered). A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the temperature range listed in section 1.3 herein. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

TABLE IA. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions $-40°C \le T_C \le +125°C$ $+3.0 V \le V_{DDD} \le +3.6 V$ $+2.25 V \le V_{DDIO} \le +2.75 V$, or $+3.0 V \le V_{DDIO} \le +3.6 V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Standby Current	I_{DDD_SB} I_{DDIO_SB}	$-40°C \le T_C \le +25°C$	1, 2, 3	All		10 1.5	mA
Standby Current	I_{DDD_SB} I_{DDIO_SB}	$25°C < T_C \le +125°C$	1, 2, 3	All		15 3	mA
Input Leakage 3/	I_{ILK}	V_{IN} = 3.6 V	1, 2, 3	All		10	µA
Output Leakage 3/	I_{OLK}	V_{OUT} = 3.6 V	1, 2, 3	All		100	µA
Low Level Output Voltage 3/	V_{OL}	V_{DDIO} = 2.25 V, I_{OL} = 6 mA V_{DDIO} = 3.00 V, I_{OL} = 6 mA	1, 2, 3	All		0.5	V
High Level Output Voltage 3/	V_{OH}	V_{DDIO} = 2.25 V, I_{OH} = -6 mA	1, 2, 3	All	1.75		V
		V_{DDIO} = 3.0 V, I_{OH} = -6 mA			2.50		
Read Operating Supply Current, Low Frequency	I_{DDDOP_R1} I_{DDIOOP_R1}	f = 1MHz, CE_B, WE = V_{SS}, OE = V_{DDIO}	1, 2, 3	All		30 10	mA
Write Operating Supply Current, Low Frequency	I_{DDDOP_W1} I_{DDIOOP_W1}	f = 1MHz, CE_B,OE = V_{SS}, WE = V_{DDIO} DQ = vector controlled	1, 2, 3	All		50 10	mA
Read Operating Supply Current, Max Frequency	I_{DDDOP_R9} I_{DDIOOP_R9}	f = 9MHz, CE_B, WE = V_{SS}, OE = V_{DDIO}	1, 2, 3	All		60 30	mA
Write Operating Supply Current, Max Frequency	I_{DDDOP_W7} I_{DDIOOP_W7}	f = 9MHz, CE_B,OE = V_{SS}, WE = V_{DDIO}, DQ = vector controlled	1, 2, 3	All		100 10	mA
Input Capacitance 4/	C_{IN}	V_{IN} = V_{DDIO} or V_{SS}, f = 1MHz	4	All		12	pF
Output Capacitance 4/	C_{OUT}	V_{IN} = V_{DDIO} or V_{SS}, f = 1MHz	4	All		15	pF
Functional tests 5/ 6/			7, 8	All			
Address Setup Time 6/	Tads	See Figures 5 & 6	9, 10, 11	All	5		ns
Address Hold Time 6/	Tadh		9, 10, 11	All	15		ns
WE Setup Time 6/	Twes		9, 10, 11	All	5		ns
WE Hold Time 6/	Tweh		9, 10, 11	All	15		ns
CE_B Setup Time 6/	Tcebs		9, 10, 11	All	5		ns
CE_B Hold Time 6/	Tcebh		9, 10, 11	All	15		ns
DQ valid with respect to rising edge of CLK 6/	Tclkdv		9, 10, 11	All	50	95	ns
CLK low to DQ Hi-z 6/	Tclkhz		9, 10, 11	All	1	15	ns
OE access time 6/	Toedv		9, 10, 11	All	1	15	ns
OE de-asserted to outputs Hi-z 6/	Toehz		9, 10, 11	All		15	ns
Read Cycle Time 7/	Tminr		9, 10, 11	All	120		ns
Data Setup Time 6/	Tdqs		9, 10, 11	All	5		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics. – Continued. 1/ 2/

Test	Symbol	Conditions $-40°C \leq T_C \leq +125°C$ $+3.0 V \leq V_{DDD} \leq +3.6 V$ $+2.25 V \leq V_{DDIO} \leq +2.75 V$, or $+3.0 V \leq V_{DDIO} \leq +3.6 V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Data Hold Time 6/	Tdqh	See Figures 5 & 6	9, 10, 11	All	15		ns
Write Cycle Time 7/	Tminw		9, 10, 11	All	140		ns
Clock Low Time 6/	Tlo		9, 10, 11	All	15		ns
Clock High Time 6/	Thi		9, 10, 11	All	15		ns
AUTOINCR Setup Time 6/	Tais_ar		9, 10, 11	All	5		ns
AUTOINCR Hold Time 6/	Taih_ar		9, 10, 11	All	15		ns
INIT, DONE, OVERFLOW_IN (Controls) Setup Time 6/	Tacs_ar		9, 10, 11	All	5		ns
INIT, DONE, OVERFLOW_IN (Controls) Hold Time 6/	Tach_ar		9, 10, 11	All	15		ns
DQ valid with respect to rising edge of CLK 6/	Tclkkdv_ar		9, 10, 11	All	50	95	ns
Rising Edge of Clock to Overflow High 6/	Tovrf_ar		9, 10, 11	All		10	ns
CE_B access time 6/	Tcebdv_ar		9, 10, 11	All		15	ns
CE_B de-asserted to outputs Hi-z 6/	Tcebhz_ar		9, 10, 11	All	1	15	ns
AUTOINCR Cycle Time 7/	Tminr_ar		9, 10, 11	All	120		ns
AUTOINCR Clock High Time 6/	Thi_ar		9, 10, 11	All	15		ns
AUTOINCR Clock Low Time 6/	Tlo_ar		9, 10, 11	All	15		ns

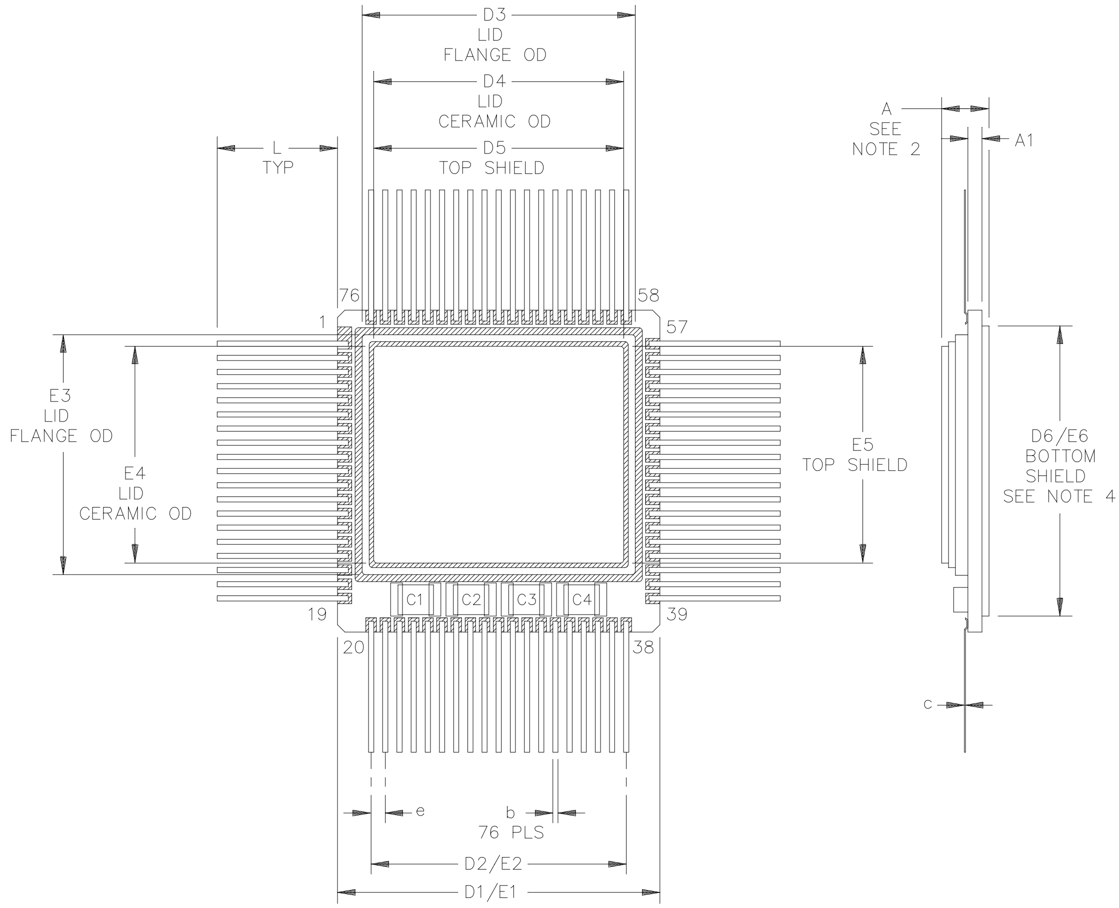
1/ Pre-irradiation values for RHA marked devices shall also be the post-irradiation values unless otherwise specified.
2/ When performing post-irradiation electrical measurements for any RHA level T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C.
3/ Applies only to pins specified for customer use.
4/ See paragraph 4.4.1.c. This parameter shall be tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in Table IA.
5/ See paragraphs 3.2.8 (including subparagraphs 3.2.8.1 and 3.2.8.2) and 4.4.1.b.
6/ See paragraphs 3.2.8.1 and 3.2.8.2.
7/ Test performed using a functional vector at the specified timing.

TABLE IB. SEP Test Limits 1/ 2/

Device Type	Particle Type	Bias V_{DDD} = 3.0V Single Event Upset Error Rate (SER) 3/ (Adam's 90% environment)	Bias V_{DDD} = 3.6V No single event latch-up (SEL) occurs at effective LET 4/
All	Heavy ion	1 $x10^{-10}$ upsets/bit-day 5/	120 MeV-cm^2/mg
All	Proton	1 $x10^{-11}$ upsets/bit-day 5/	-

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Power Supply = the worst case of the min and max of the Power Supply range defined in 4.4.4.4 herein. Temperature = the worst case of the min and max of the Temperature range defined in 4.4.4.4 herein.
4/ Power Supply = the max of the Power Supply range defined in 4.4.4.4 herein. Temperature = the max of the Temperature range defined in 4.4.4.4 herein.
5/ Projected performance based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield using Weibull parameters based on an analysis of test data (see 4.4.4.4) and simulation results. Weibull parameters and other relevant attributes are available from the vendor upon request to calculate projected upset rate performance for other orbits and environments.

Case X



1. Controlling dimensions are in millimeters, inches dimensions are given for reference only.
2. Dimension A is the total thickness of the top shield, lid, seal ring, ceramic body, bottom shield, and shield adhesives.
3. Not applicable to this case outline.
4. The bottom shield is square and dimension E6 represents dimensions D6 and E6.

FIGURE 1. Case outline.

Case X – Continued

Symbol	Millimeters				Inches		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	3.913	4.253	4.713		.154	.167	.186
A1	1.282	1.422	1.562		.050	.056	.062
b	0.36	0.41	0.46		0.14	.016	.018
c	0.10	0.15	0.20		.004	.006	.008
D1/E1	28.91	29.21	29.51		1.138	1.150	1.162
D2/E2	---	22.86	---		---	.900	---
D3	24.743	24.943	25.143		.974	.982	.990
D4	22.711	22.911	23.111		.894	.902	.910
D5	25.581	22.708	22.835		.889	.894	.899
E3	21.517	21.717	21.917		.847	.855	.863
E4	19.482	19.685	19.885		.767	.775	.783
E5	19.355	19.482	19.609		.762	.767	.772
D6/E6	26.543	26.670	26.797		1.045	1.050	1.055
e	---	1.27	---		---	.050	---
L1	10.160	10.414	10.668		.400	.410	.420

NOTE: The package is assembled with four on-package CDR33 chip capacitors 0.1uF with 50V rating which meet approved criteria and are similar to MIL-PRF-123 capacitors. Two capacitors placed between V_{DDD} and V_{SS}, and two capacitors between V_{DDIO} and V_{SS} improve noise sensitivity for I/O switching and dose rate hardness. A is height of package including the capacitors.

FIGURE 1. Case outline – Continued.

Package Pin Number	Function	Package Pin Number	Function
1	V_{SS}	39	V_{SS}
2	TESTIN1 (V_{SS}) 1/	40	DQ12
3	TESTIN2 (V_{DDIO}) 1/	41	DQ13
4	TESTIN3 (V_{SS}) 1/	42	DQ14
5	DQ3	43	DQ15
6	V_{DDIO}	44	V_{DDIO}
7	DQ2	45	TESTOUT5 2/
8	TESTOUT1 2/	46	A19
9	TESTOUT2 2/	47	A17
10	TESTOUT3 2/	48	TESTOUT6 2/
11	TESTOUT4 2/	49	A18
12	DQ5	50	A20
13	DQ6	51	DQ11
14	V_{DDD}	52	V_{DDD}
15	DQ7	53	DQ10
16	TESTIN4 (V_{SS}) 1/	54	DQ9
17	TESTIN5 (V_{SS}) 1/	55	DQ8
18	TESTIN6 (V_{SS}) 1/	56	TESTOUT7 2/
19	V_{SS}	57	V_{SS}
20	V_{SS}	58	V_{SS}
21	DQ4	59	A16
22	OVERFLOW_O	60	A14
23	OVERFLOW_I	61	A12
24	A1	62	A10
25	V_{DDIO}	63	V_{DDIO}
26	A3	64	A8
27	A5	65	A6
28	A7	66	CLK
29	A9	67	WE
30	CE_B	68	A4
31	OE	69	A2
32	INIT	70	AUTO_INCR
33	V_{DDD}	71	V_{DDD}
34	DONE	72	X8
35	A11	73	A0
36	A13	74	DQ0
37	A15	75	DQ1
38	V_{SS}	76	V_{SS}

1/ This input signal is for the manufacturer's use only. This pin must be connected as shown in the parentheses.

2/ This output signal is for the manufacturer's use only. This pin must be left unconnected.

FIGURE 2. Terminal connections.

Functional

CLK	CE_B	WE	AUTO_INCR	INIT	DONE	OVERFLOW_IN	Function
R	0	0	0	X	X	X	Read Cycle
R	0	1	0	X	X	X	Write Cycle
R	1	X	X	X	X	X	Chip Disable
R	0	X	1	1	0	1	Read Cycle 1/
R	X	X	1	0	X	X	Chip Disable 1/
R	X	X	1	X	1	X	Chip Disable 1/
R	X	X	1	X	X	0	Chip Disable 1/

1/ Auto increment functions

Output Driver

Function	CLK	OE	CE_B	Data Outputs
Read Cycle	1	1	X	Active 1/
Read Cycle	1	0	X	Hi-Z
Read Cycle	0	X	X	Hi-Z
Write Cycle	X	X	X	Hi-Z
Chip Disable	X	X	X	Hi-Z
Auto Increment Read Cycle	X	X	0	Active
Auto Increment Read Cycle	X	X	1	Hi-Z

1/ Will become active only after sense amp operation is complete.

NOTE: For all truth tables, TESTIN* pins must be in the states shown in the Figure 2.

FIGURE 3. Truth tables.

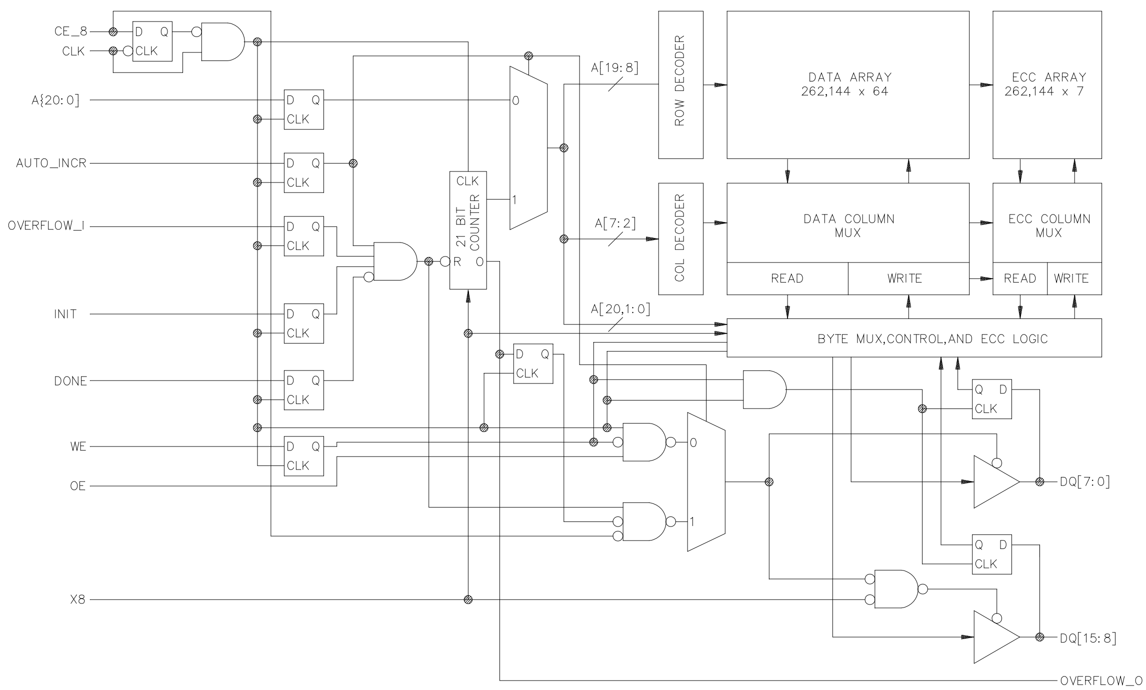
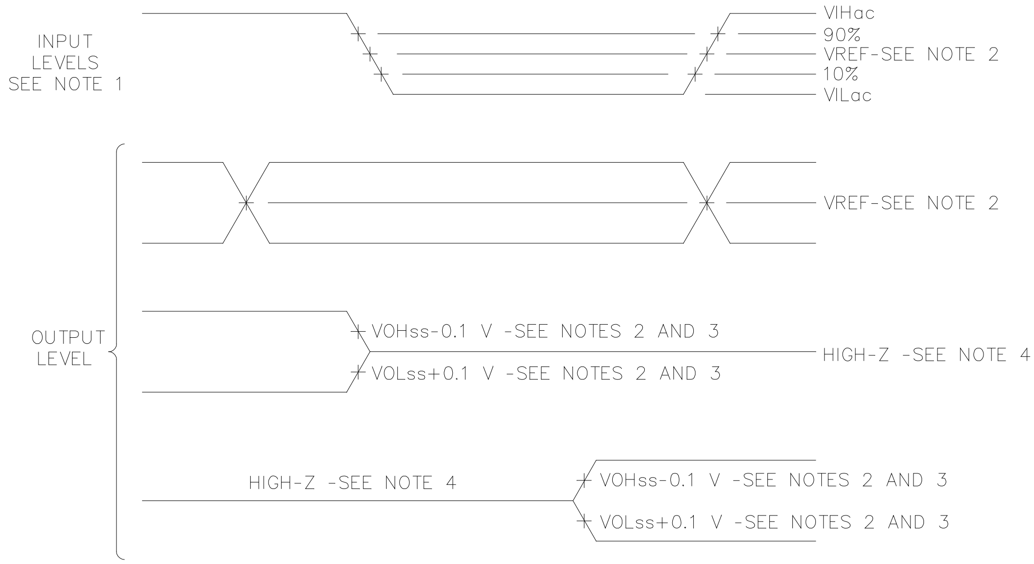
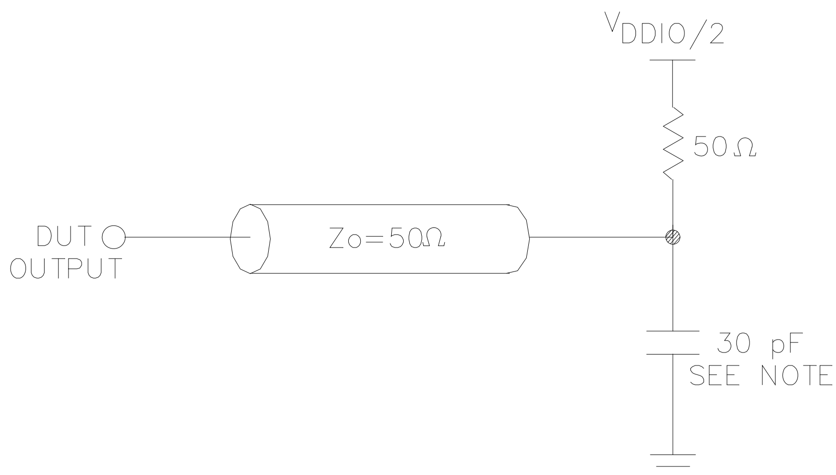


FIGURE 4. Block diagram.

TIMING INPUT / OUTPUT REFERENCES



Notes:
1. (1) Input rise and fall times = 1 ns between 90% and 10% levels.
2. (2) Timing parameter reference voltage level.
3. (3) ss: Low-Z VOH and VOL steady-state output voltage.
4. (4) High-Z output pin pulled to VLOAD by Reference Load Circuit.

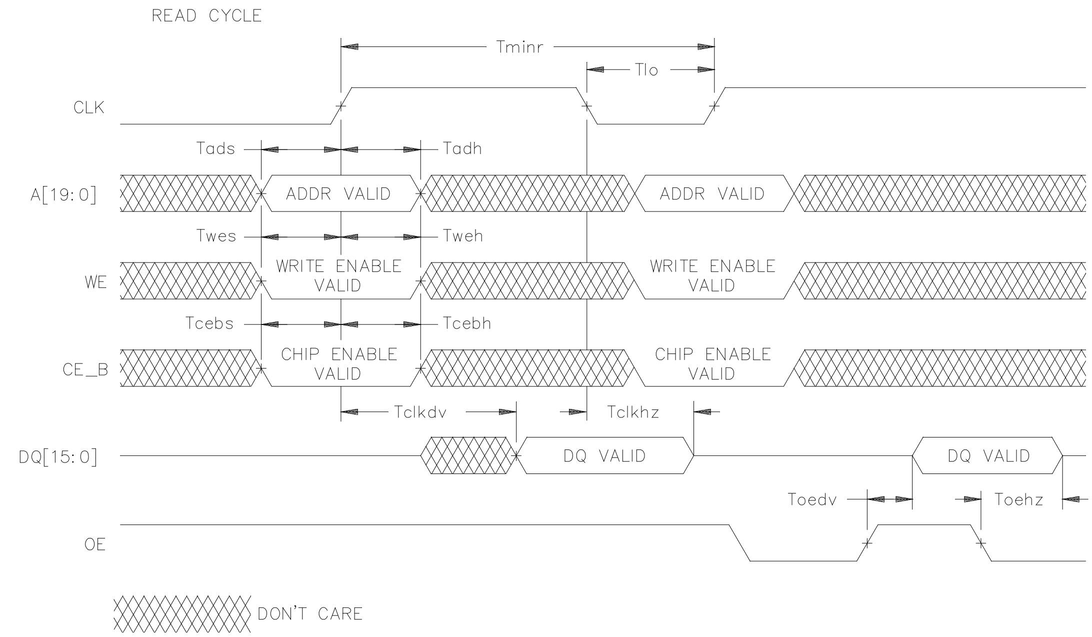


NOTE: Set to 5pF for t*hz (Low-Z to High-Z) timing parameters

I/O Type	VIHac	VILac	VREF	VLOAD
2.5 V or 3.3V CMOS	V_{DDIO}	VSS	V_{DDIO} /2	V_{DDIO} /2

FIGURE 5. Output load circuit.

Read Cycle Timing



Read Cycle Timing Auto-Increment Mode

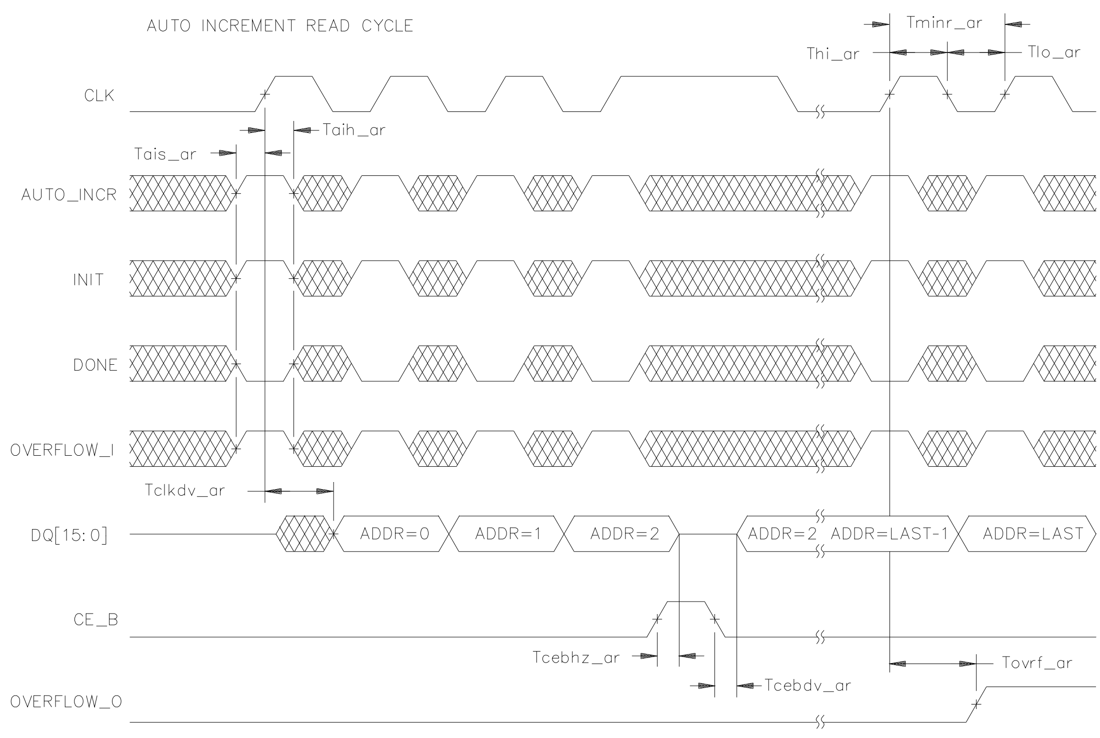
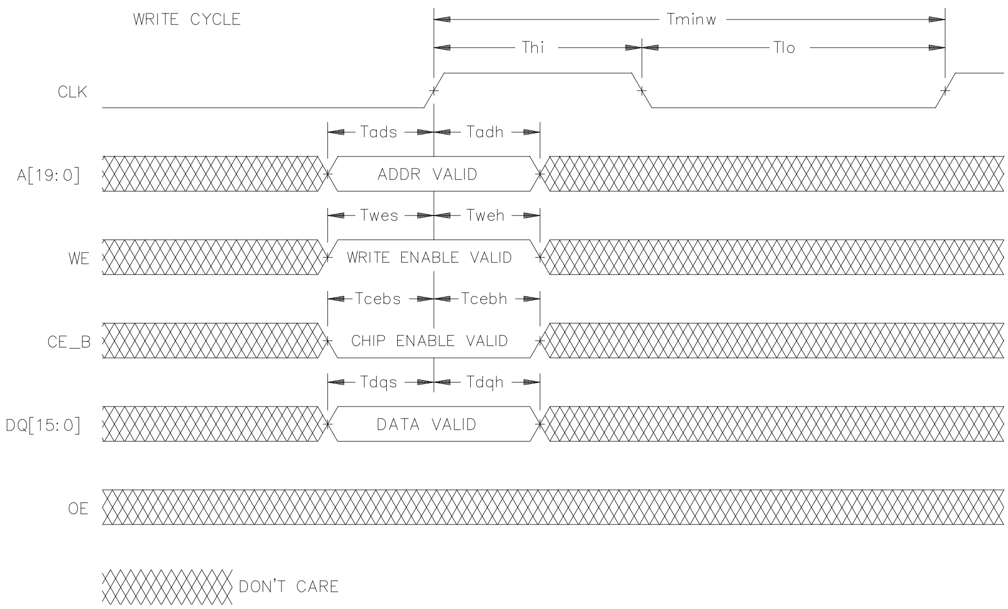


FIGURE 6. Timing waveforms.

Write Cycle Timing



Power-Up/Down Sequence

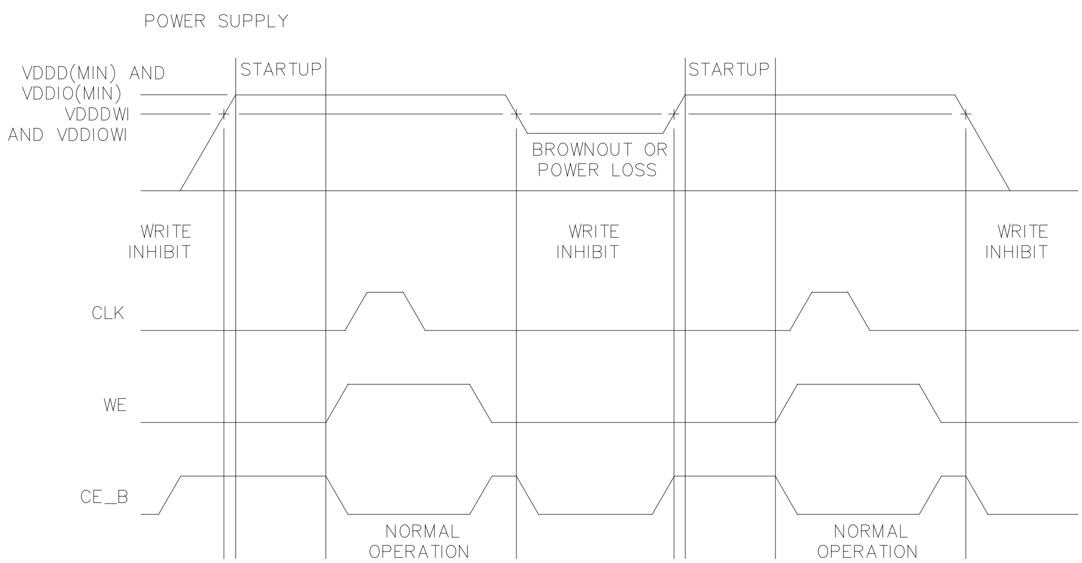


FIGURE 6. Timing waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. Capacitors are added to the package after mechanical screening.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device class Q shall be done per approved QM plan and include:
(1) Internal visual, TM 2010 condition A
(2) X-ray (top view only)
(3) PIND
(4) Serialization
(5) 240-hour dynamic burn-in, delta, read and record (in place of standard class Q burn-in)
(6) Static Burn-in, delta, read and record

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Pre burn-in electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Dynamic burn-in (method 1015)	Required	Required
Interim electrical parameters (see 4.2)	Not Applicable	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11, Δ 1/ 2/
Static burn-in (method 1015)	Not Required	Required
Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 1/	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11, Δ 1/ 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11 3/	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11 3/
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ 2/
Group D end-point electrical parameters (see 4.4)	1, 7	1, 7 4/
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameter tests.
3/ See paragraph 4.4.1.
4/ See paragraph 4.4.3.

TABLE IIB. Burn-In and operating life test delta parameters (25ºC).

Symbol	**Parameter**	**Delta limits 1/ 2/**
$I_{DD\ SB}$	V_{DDD} Standby Current	±10% or 1 mA, whichever is greater
I_{ILK}	Input Leakage Current	±1 µA
I_{OLK}	Output Leakage Current	±10 µA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ Parameter shifts for leakage parameters are calculated at +25°C only.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. The sample size for Group D Subgroups 3 through 5 shall be 5(0) with acceptance on zero failures.

a. End-point electrical test shall occur prior to magnetic shield removal. Electrical testing after shield removal may result in functional failures induced by stray magnetic fields.

b. Fine and Gross Leak testing shall be performed after magnetic shield removal. Failure to remove magnetic shields prior to leak testing may result in false failures caused by the presence of the magnetic shield adhesive. This applies to all methods of leak testing specified in MIL-STD-883, Method 1014, including Condition B1 radioisotope fine leak.

c. MIL-STD-883, Method 1018 shall be performed after magnetic shield removal. Failure to remove magnetic shields prior to RGA may result in false failures caused by the presence of the magnetic shield adhesive.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed in accordance with MIL-STD-883 method 1019, and as specified herein. The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.2 Dose rate induced latch-up testing. When specified by the procuring activity, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When specified by the procuring activity, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be ≥ than 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C±10ºC. The latchup test temperature shall be at the maximum rated operating temperature ±10°C.

f. The Power Supply shall be within the recommended operating range.

g. For SEP test limits see Table IB herein.

h. Testing shall be performed using True and Complement or other test patterns that sensitize the part to possible upsets caused by particles interacting with the circuitry.

4.4.4.5 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein (see 1.6). All device classes must meet the post irradiation end-point electrical parameter limits as defined in Table IA, for the subgroups specified in Table IIA herein at T_A = +25°C ± 5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.5 Delta measurements for device class V. Delta measurements, as specified in Table IIB, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta limit compliance. The electrical parameters to be measured, with associated delta limits are listed in Table IIB.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied::

a. RHA test conditions (TID, DRU, DRS, and SEP).

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latch-up (SEL).

6.8 Package Shield Information. Fine and Gross Leak testing shall be performed after magnetic shield removal. Internal Water Vapor Content shall be performed after magnetic shield removal. Failure to remove magnetic shields prior to leak testing or RGA may result in false failures due to absorption by the shield adhesive. Contact the manufacturer for shield removal process instructions.

6.9 Signal definitions.

CLK	Rising edge initiates an access of memory. A(20:0), WE and DQ(15:0) are latched on the rising edge. High level required for DQ(15:0) outputs to be enabled.
CE_B	Active low chip enable. High state at rising edge of clk disables chip (no memory access and outputs go to Hi-Z). Low state at rising edge enables an access of the memory.
A(20:0)	Address Word Input. A(20) is MSB, A(0) is LSB. In 16 bit configuration, A(20) is not used and should be tied to V_{SS} .
DQ(15:0)	Data Input/Output Signals. Bi-directional data pins which serve as data outputs during a read operation and as data inputs during a write operation. When in X8 mode, only DQ(7:0) are active and DQ(15:8) pins should be tied to VSS.
WE	Write Enable. Active high write enable. High state at rising edge of CLK initiates a write cycle. Low state at rising edge of CLK initiates a read cycle.
OE	Output Enable. Active high output enable.
X8	Byte Mode Configuration Pin. Active high input. Configures the memory interface as 8 bit when high (DQ(7:0) only active). When low, memory interface is 16 bits (DQ(15:0)). Should be tied directly to V_{SS} or V_{DDIO} depending on desired configuration.
AUTO_INCR	Auto Increment Mode Enable. Active high input sampled on rising edge of CLK. When high enables internal address counter and read only mode.
OVERFLOW_I	Counter Enable Input Pin. Active High Enable for internal counter (when INIT=1,DONE=0). Used to daisy chain devices.
INIT	Active High Interface Pin used to reset internal address counter (when OVERFLOW I=1, DONE=0)
DONE	Active Low Interface Pin used to reset internal address counter (when OVERFLOW I=1, INIT=1).
OVERFLOW_O	Internal Overflow Counter Indicator. Active high output signal indicates internal counter has reached last address. Used to daisy chain devices.
V_{SS}	Ground
V_{DDD}	DC Power Source Input: nominal 3.30 V
V_{DDIO}	DC I/O Power Source Input: nominal 2.50 V or 3.30 V
TESTINx	These are test input pins and should not be used by the customers. Connect as defined in FIGURE 2 Terminal Connections diagram to either V_{SS} or V_{DDIO}.
TESTOUTx	These pins shall be treated as "no connects" and have no connection on the circuit board.

APPENDIX A

Appendix A forms a part of SMD 5962-13212

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.1.1.1 Functional Test Conditions. VIH and VIL levels during functional testing shall comply with the requirements of 3.2.8 herein.

A.1.1.2 Functional Test Sequence. Functional test patterns may be performed in any order.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Increment address from minimum to maximum writing each address with solid 0.
Step 2. Increment address from minimum to maximum while performing 2a and 2b.
Step 2a. Read and verify an address.
Step 2b. Write the address with complement data.
Step 3. Increment address from minimum to maximum while performing 3a.
Step 3a. Read and verify an address.
Step 4. Increment address from minimum to maximum while performing 4a, 4b, 4c, and 4d.
Step 4a. Read and verify the address.
Step 4b. Write the address with complement data.
Step 4c. Read and verify the address
Step 4d. Write the address with complement data.
Step 5. Decrement address from maximum to minimum while performing 5a and 5b.
Step 5a. Read and verify the address.
Step 5b. Write the address with complement data.
Step 6. Decrement address from maximum to minimum while performing 6a, 6b, 6c, and 6d.
Step 6a. Read and verify the address.
Step 6b. Write the address with complement data.
Step 6c. Read and verify the address
Step 6d. Write the address with complement data.
Step 7. Decrement address from maximum to minimum while performing 7a.
Step 7a. Read and verify an address.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 Solids.

Step1. Write x00 data pattern to all addresses from minimum to maximum.
Step 2. Read and verify x00 data pattern at all addresses.
Step 3. Write xFF data pattern to all addresses from minimum to maximum.
Step 4. Read and verify xFF data pattern at all addresses.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Control signals functional Verification.

Each test performed independently.
OE: Output Driver Truth Table
CE_B: Chip Disable
AI_X8: Auto Increment x8 Mode
AI_X16: Auto Increment x16 Mode

A.3.5 Other Functional Testing.

A.3.5.1 Voltage Regulator tests. See paragraph 3.2.8.1.

A.3.5.2 Error Correction Circuitry (ECC) tests. See paragraph 3.2.8.2.

A.3.5.3 Non-Volatility tests. See paragraph 3.2.8.3.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-03-21

Approved sources of supply for SMD 5962-13212 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H1321201VXC	34168	HXNV01600AVH
5962H1321201QXC	34168	HXNV01600AWH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell Aerospace 12001 Highway 55 Plymouth, MN 55441