REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated to current MIL-PRF-38535 requirements. Corrected the 2.3 V ≤ V_{DDD} ≤ 2.7 V maximum limit for t_{BLQV} and t_{GLQV} in table IA. Corrected test conditions for $I_{DDDOPR1}$ and $I_{DDDOPR40}$. Corrected subscripts in symbols I_{ILK} and I_{OLK} in table IIB. Corrected 6.7 for CE, VDD and VDDD. - lhl	13-12-11	Charles F. Saffle
B	Changed V_{DD}/V_{DDD} Voltage Ramp Time in 1.4. Added Heavy ion no SEL in 1.6. Corrected Conditions in table IA. Added additional V_{OL} and V_{OH} conditions to table IA. Corrected NBE capacitance in table IA. Corrected table IB footnotes. Corrected footnote 2 of figure 1. Corrected figures 3 and 4. Updated timing transition waveform and updated write timing waveform to figure 5. Corrected 6.7 for NCS and added V_{SS}. Updated drawing to current MIL-PRF-38535 requirements. - lhl	14-03-12	Charles F. Saffle
C	Added footnote in 1.2.2 for device type 01. Corrected 1.4 for V_{IH} and V_{IL}. Corrected 1.6 for Dose rate induced upset and survivability. Updated 3.2.6 and sequence through 3.2.9. Added Figure 6 block diagram. Added minimum limit for V_{OH} in table IA. Added additional screening to 4.2.1. Corrected table IIA for device class Q - llb	14-12-04	Charles F. Saffle

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
13-03-22

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2M X 32-BIT (64Mb), RADIATION-HARDENED, SRAM, MULTI-CHIP MODULE

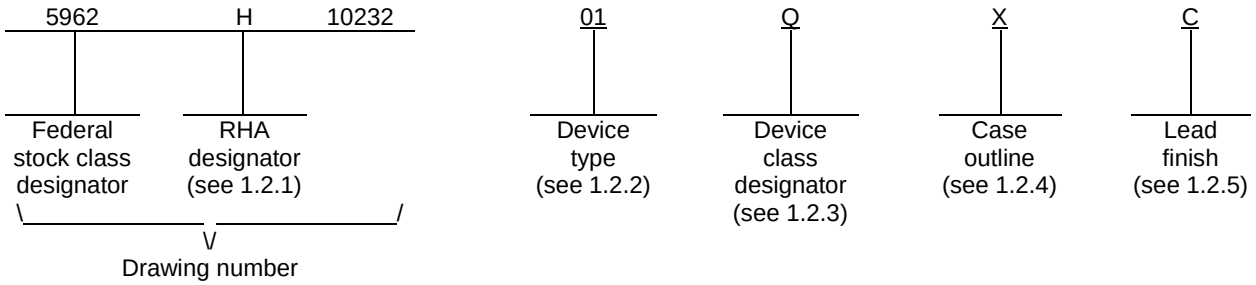
SIZE	CAGE CODE	
A	**67268**	**5962-10232**

SHEET 1 OF 24

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HXSR06432	2M X 32-bit rad-hard CMOS SRAM 1/

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	86	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q and V.

1/ Device type 01, when provided as class Q, will have additional testing as defined in section 4.2.1.d.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range I/O (V_{DDD})	-0.5 V dc to +4.4 V dc
Supply voltage range Core (V_{DD})	-0.5 V dc to +2.4 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{DDD} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{DDD} + 0.5 V dc
DC or average output current (I_{OUT})	15 mA
Storage temperature	-65°C to +150°C
Lead temperature (soldering 5 seconds)	+270°C
Thermal resistance, junction to case (Θ_{JC})	5.0°C /W
Voltage applied to pins, except power	-0.5 V dc to V_{DDD} + 0.5V dc
Maximum power dissipation	2.5 W
Case operating temperature range (T_C)	-55°C to +125°C
Maximum junction temperature (T_J)	175°C

1.4 Recommended operating conditions. 3/

Supply voltage range I/O (V_{DDD})	3.0 V dc to 3.6 V dc
Optional Supply voltage range I/O (V_{DDD})	2.3 V dc to 2.7 V dc
Supply voltage range Core (V_{DD})	1.65 V dc to 1.95 V dc
Supply voltage reference (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	0.7 x V_{DDD} to V_{DDD} + 0.3 V dc
Low level input voltage range (V_{IL})	-0.3 V dc to 0.3 x V_{DDD}
Voltage on any pin (V_{IN})	-0.3 V dc to V_{DDD} + 0.3
Power Down Time	5 ms minimum 4/
Case operating temperature range (T_C)	-55°C to +125°C
V_{DD}/V_{DDD} Voltage Ramp Time	1 x 10^{-5} to 1.0 second

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

1.6 Radiation features. 5/

Maximum total dose available (dose rate = 50-300 rad(Si)/s)	1 x 10^6 Rads(Si)
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.4)	≤ 120 MeV-cm^2/mg
Heavy Ion Single event upset (SEU) rate	1 x 10^{-12} upsets/bit-day 6/
Proton Single event upset (SEU) rate	2 x 10^{-12} upsets/bit-day 6/
Neutron irradiation	1 x 10^{14} neutrons/cm^2 7/
Dose rate induced upset	1 x 10^{10} Rad(Si)/sec for < 20 nsec
Dose rate survivability	1 x 10^{12} Rad(Si)/sec for < 20 nsec
Latch-up	Immune by SOI technology

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltages are referenced to V_{SS}.

3/ Maximum applied voltage shall not exceed 4.4 V.

4/ If the SRAM is powered down, the power must remain turned off for the “Power Down Time” before turned back on.

5/ Radiation features and test limits specified herein based on 16Mb single chip SRAM test results (5962-08202/08203). For details on these RHA parameters and test results, contact the device manufacturer.

6/ Projected performance based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield using Weibull parameters derived from actual test data (see 4.4.4.4). Weibull parameters are available from vendor to calculate upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).

7/ Guaranteed but not tested for 1MeV equivalent neutrons.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Block diagrams. The block diagrams shall be as specified on figure 6.

3.2.7 Radiation test circuit The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.8 Functional tests. Various functional tests used to test this device are contained in appendix A (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.9 Signal definitions. The signal definitions shall be as specified in 6.7 herein.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in Table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in Table IIA. The electrical tests for each subgroup are defined in Table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 External decoupling capacitors. The CDR33 chip capacitors are mounted to the outside lid of the package. Ceramic capacitors shall meet approved criteria (design, screening and testing) in accordance with MIL-PRF-123 or as approved by the Qualifying Activity. The capacitors are included to improve the noise sensitivity for I/O switching and dose rate hardness.

TABLE IA. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ $1.65\ V \le V_{DD} \le 1.95\ V$ unless otherwise specified	Group A Sub-groups	Device type	Limits		Unit
					Min	Max	
Standby Current – NCS disabled	I_{DDSB02} $I_{DDDSB02}$	f=0MHz, NCS(0-3), NOE, NWE = V_{DDD}	1, 2, 3	01		120.0 1.2	mA
Standby Current – enabled	I_{DDSB} I_{DDDSB}	f=0MHz, NCS 2/, NOE, NWE = V_{SS}	1, 2, 3	01		120.0 1.2	mA
Operating Supply Current Disabled, address bus at max frequency 3/	I_{DDOP3} I_{DDDOP3}	f=40MHz, NCS(0-3), NOE, NWE = V_{DDD}	1, 2, 3	01		8 20	mA
Operating Supply Current Deselected, write mode 3/	I_{DDOP1} I_{DDDOP1}	NCS and NOE = V_{DDD}, NWE at 1MHz vector controlled	1, 2, 3	01		0.4 0.8	mA
Operating Supply Current Selected, write mode low frequency 3/	I_{DDOPW1} $I_{DDDOPW1}$	f=1MHz, NCS*=V_{SS}, NOE=V_{DDD}, NWE vector controlled	1, 2, 3	01		5.6 0.95	mA
Operating Supply Current Selected, write mode high frequency 3/	$I_{DDOPW40}$ $I_{DDDOPW40}$	f=40MHz, NCS*=V_{SS}, NOE=V_{DDD}, NWE vector controlled	1, 2, 3	01		200.3 29.0	mA
Operating Supply Current Selected, read mode low frequency 3/	I_{DDOPR1} $I_{DDDOPR1}$	f=1MHz, NCS*=V_{SS}, NOE, NWE =V_{DDD}	1, 2, 3	01		3.0 0.8	mA
Operating Supply Current Selected, read mode high frequency 3/	$I_{DDOPR40}$ $I_{DDDOPR40}$	f=40MHz, NCS*=V_{SS}, NOE, NWE =V_{DDD}	1, 2, 3	01		80.3 23.0	mA
Data Retention Current	I_{DR1} I_{DR2}	V_{DD} = 1.0 V V_{DDD} = 2.0 V	1, 2, 3	01		80 0.8	mA
Low level output voltage	V_{OL}	V_{DDD} = 3.0 V, V_{DD} = 1.65 V, I_{OL}=10mA, V_{IL} =V_{SS}, V_{IH} = V_{DDD}	1, 2, 3	01		0.4	V
		V_{DDD} = 2.3 V, V_{DD} =1.65 V, I_{OH}= 10mA, V_{IL} = V_{SS}, V_{IH} = V_{DDD} 6/					
High level output voltage	V_{OH}	V_{DDD} = 3.0 V, V_{DD} =1.65 V, I_{OH}=-5mA, V_{IL} = V_{SS}, V_{IH} = V_{DDD}	1, 2, 3	01	2.7		V
		V_{DDD} = 2.3 V, V_{DD} = 1.65 V, I_{OL} = 5mA, V_{IL} =V_{SS}, V_{IH} = V_{DDD} 6/			2		
Input leakage current	I_{ILK}	V_{IN} = 3.6 V, V_{DDD} = 3.6 V, V_{DD} = 1.95 V all other pins at 3.6 V	1, 2, 3	01	-10	10	µA
Output leakage current	I_{OLK}	V_{OUT} = 3.6V, V_{DDD} = 3.6 V, V_{DD} = 1.95 V all other pins at 3.6 V	1, 2, 3	01	-20	20	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ or $2.3\ V \le V_{DDD} \le 2.7\ V$ $1.65\ V \le V_{DD} \le 1.95\ V$ $V_{IH}=V_{DDD}$, $V_{IL}=V_{SS}$ unless otherwise specified See figures 4 and 5	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address capacitance 4/ NCS input capacitance NOE input capacitance CE input capacitance NWE input capacitance NBE input capacitance	C_A C_{NCS} C_{NOE} C_{CE} C_{NWE} C_{NBE}	$V_{IN} = V_{DDD}$ or V_{SS}, f = 1 MHz See 4.4.1e	4	01		25 25 35 35 35 25	pF
Data I/O capacitance 4/	C_{DQ}		4	01		25	pF
Functional tests		See 3.2.7 and 4.4.1.c	7, 8	01			
Data retention voltage	V_{DR}	V_{DDD} = 2.0 V, V_{DD} = 1.0 V	7, 8	01	5/		
Read cycle time	t_{AVAVR}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	20 22		ns
Address access time	t_{AVQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		20 22	ns
Address change output invalid time	t_{AXQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	4 4		ns
Chip select access time	t_{SLQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		21 22	ns
Chip select to output enable time	t_{SLQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Chip select to output disable time	t_{SHQZ}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		4.5 4.5	ns
Chip enable access time	t_{EHQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		21 22	ns
Chip enable to output enable time	t_{EHQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Chip enable to output disable time	t_{ELQZ}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		6.0 6.0	ns
Byte enable access time	t_{BLQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		6 7	ns
Byte enable to output active time	t_{BLQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Byte enable to output disable time	t_{BHQZ}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		4.3 4.3	ns
Output enable access time	t_{GLQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		6.5 7.5	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ or $2.3\ V \le V_{DDD} \le 2.7\ V$ $1.65\ V \le V_{DD} \le 1.95\ V$ $V_{IH}=V_{DDD}$, $V_{IL}=V_{SS}$ unless otherwise specified See figures 4 and 5	Group A subgroups	Device type	Limits		Test
					Min	Max	
Output enable to output active time	t_{GLQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Output enable to output disable time	t_{GHQZ}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		4.8 4.8	ns
Write cycle time	t_{AVAVW}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	15 15		ns
Minimum write enable pulse width	t_{WLWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	7 7		ns
Chip select to end of write time	t_{SLWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	10 10		ns
Chip enable to end of write time	t_{EHWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	10 10		ns
Data valid to end of write time	t_{DVWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	6 6		ns
Address valid to end of write time	t_{AVWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	12 12		ns
Data hold time after end of write time	t_{WHDX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Address valid setup to start of write time	t_{AVWL}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Address valid hold after end of write time	t_{WHAX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Write enable to output disable time	t_{WLQZ}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		6.0 6.0	ns
Write disable to output enable time	t_{WHQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Write disable write enable pulse width 6/	t_{WHWL}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	5 5		ns
Byte enable to end of write time	t_{BLWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	10 10		ns
Byte enable pulse width	t_{BLBH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	8		ns
Write enable to end of byte enable	t_{WLBH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	8		ns
Data valid to end of byte enable	t_{DVBH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	8		ns
Data hold time after end of byte enable	t_{BHDX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued. 1/

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, R, and H of irradiation. However, this device is only tested at the 'H' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A= +25°C.
2/ Vector controlled, only one NCS[0-3] at 0 volts.
3/ These dynamic operating mode current measurement s ($I_{DDOPx\ and}$ I_{DDDOPx}) exclude standby mode currents ($I_{DDS\ and}$ I_{DDDS}).
4/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in Table IA.
5/ As verified by functional tests.
6/ Guaranteed to the limits specified in Table IA, but not tested.

TABLE IB. SEP Test Limits. 1/ 2/ 3/

Device Type	ION Type	Memory pattern	Bias V_{DD} = 1.65 V SEU Rate Adam's 90% environment 4/	Bias V_{DD} =1.95 V No latch-up (SEL) Effective LET
01	Heavy ion	5/	1×10^{-12} upsets/bit-day 6/	LET ≤ 120 MeV/mg/cm^2
01	Proton	5/	2×10^{-12} upsets/bit-day 6/	-

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ For SEL worst case temperature T_A = +125°C ± 10°C and for SEU worst case temperature T_A = +25°C ± 10°C.
4/ Projected performance based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield using Weibull parameters derived from actual test data(see 4.4.4.4). Weibull parameters are available from vendor to calculate upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).
5/ Testing shall be performed using checkerboard and checkerboard bar test patterns.
6/ The proton test is performed at the energy level 200 MeV and observed SEU rate is less than geosynchronous orbits/environments program goal SEU rate = 2×10^{-12} errors/bit-day. CRÈME 96 with Weibull parameters are available from the vendor upon request.

Case outline X

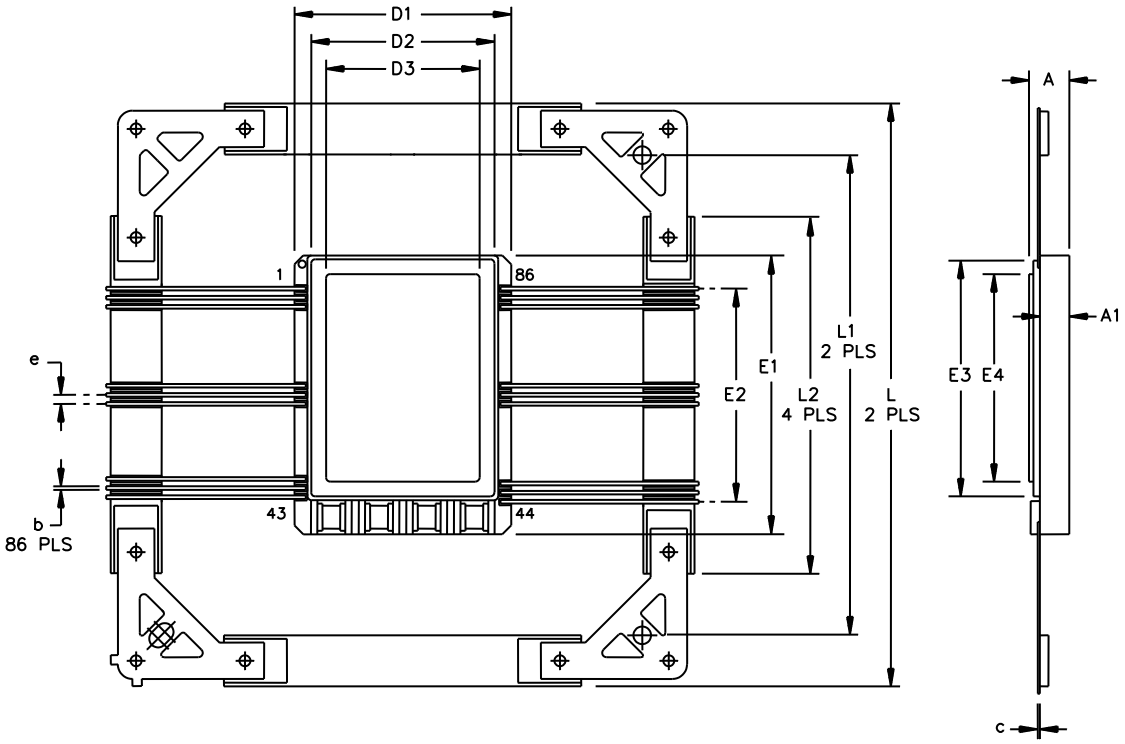


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE **A**		**5962-10232**
		REVISION LEVEL C	SHEET 10

Symbol	mm	
	min	max
A	4.34	5.20
A1	3.15	3.85
b	0.15	0.25
c	0.125	0.20
D1	24.25	24.73
D2	20.83	21.08
D3	17.53	17.78
E1	30.93	31.55
E2	26.54	26.80
E3	26.67	26.92
E4	23.37	23.62
e	.585	.685
L	62.99	64.01
L1	54.23	54.49
L2	42.75	43.61

NOTES:

1. Lid is electrically connected to V_{SS}.
2. The package is assembled with four on package CDR33 chip capacitors 0.1uF with 50V rating which meet approved criteria and are similar to MIL-PRF-123 capacitors. Two capacitors placed between V_{DD} and V_{SS} and two between V_{DDD} and V_{SS} to improve noise sensitivity for I/O switching and dose rate hardness.

FIGURE 1. Case outline - Continued.

Device types	All		
Case outlines	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	Cathode	86	Anode
2	V_{SS}	85	V_{SS}
3	V_{DD}	84	V_{DD}
4	A0	83	A18
5	A1	82	A17
6	A2	81	A16
7	A3	80	V_{SS}
8	A4	79	V_{DDD}
9	V_{SS}	78	DQ31
10	V_{DDD}	77	DQ30
11	DQ0	76	DQ29
12	DQ1	75	DQ28
13	DQ2	74	DQ27
14	DQ3	73	DQ26
15	DQ4	72	NOE
16	DQ5	71	V_{DDD}
17	V_{SS}	70	NBE3
18	V_{DDD}	69	NCS3
19	NBE0	68	DQ25
20	NCS0	67	DQ24
21	DQ6	66	DQ23
22	DQ7	65	DQ22
23	DQ8	64	NCS2
24	DQ9	63	CE
25	NCS1	62	NBE2
26	NBE1	61	V_{DDD}
27	V_{DDD}	60	V_{SS}
28	NWE	59	DQ21
29	DQ10	58	DQ20
30	DQ11	57	DQ19
31	DQ12	56	DQ18
32	DQ13	55	DQ17
33	DQ14	54	DQ16
34	DQ15	53	V_{DDD}
35	V_{DDD}	52	V_{SS}
36	V_{SS}	51	A15
37	A5	50	A14
38	A6	49	A13
39	A7	48	A12
40	A8	47	A11
41	A9	46	A10
42	V_{DD}	45	V_{DD}
43	V_{SS}	44	V_{SS}

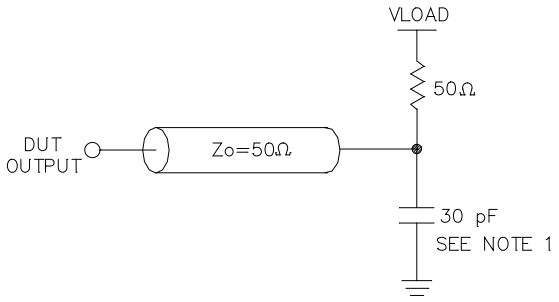
FIGURE 2. Terminal connections.

CE	NCS*				NWE	NOE	NBE				MODE	D			
	0	1	2	3			0	1	2	3		0-7	8-15	16-23	24-31
L	X	X	X	X	X	X	X	X	X	X	Disable	Hi-Z	Hi-Z	Hi-Z	Hi-Z
X	H	H	H	H	X	X	X	X	X	X	De-select	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	L	H	H	H	H	H	X	X	X	X	Read Standby	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	L	H	H	H	H	X	H	H	H	H	Read Standby	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	L	H	H	H	H	L	L	H	H	H	Read Data Out	DO	Hi-Z	Hi-Z	Hi-Z
H	L	H	H	H	H	L	H	L	H	H	Read Data Out	Hi-Z	DO	Hi-Z	Hi-Z
H	L	H	H	H	H	L	H	H	L	H	Read Data Out	Hi-Z	Hi-Z	DO	Hi-Z
H	L	H	H	H	H	L	H	H	H	L	Read Data Out	Hi-Z	Hi-Z	Hi-Z	DO
H	L	H	H	H	H	L	L	L	L	L	Read Data Out	DO	DO	DO	DO
H	L	H	H	H	L	X	H	H	H	H	No Write	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	L	H	H	H	L	H	L	H	H	H	Write	DI	X	X	X
H	L	H	H	H	L	H	H	L	H	H	Write	X	DI	X	X
H	L	H	H	H	L	H	H	H	L	H	Write	X	X	DI	X
H	L	H	H	H	L	H	H	H	H	L	Write	X	X	X	DI
H	L	H	H	H	L	H	L	L	L	L	Write	DI	DI	DI	DI

Note: L=low, H=high, X=low or high, Hi-Z = Hi Impedance, DO = Data Output and DI = Data Input.
NOE = H: High Z output state maintained for NCS = X, CE = X, NWE = X*NCS(0-3).
Only one NCS can be L, others remain H.

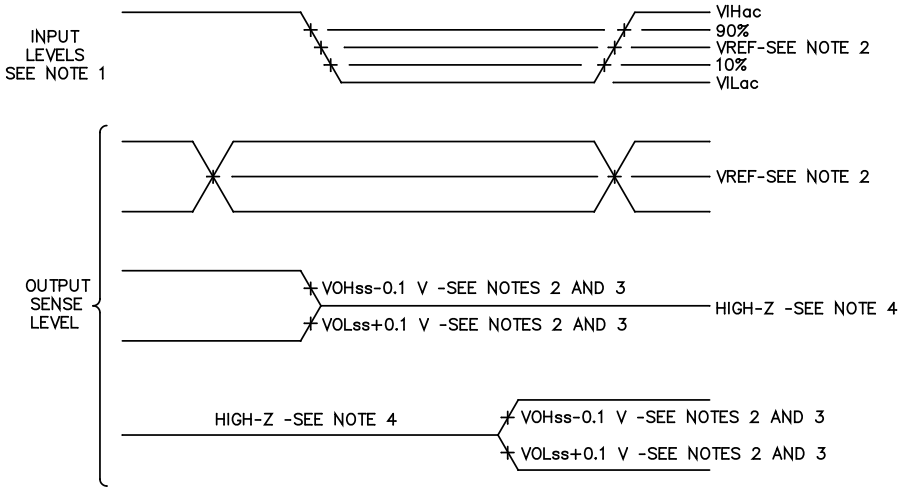
FIGURE 3. Truth table.

AC Timing Output Load Circuit



NOTE 1: Set to 5 pF for T*QZ (Low-Z to High-Z) timing parameters.

I/O	VLOAD
3.3 V	$V_{DDD}/2$
2.5 V	$V_{DDD}/2$

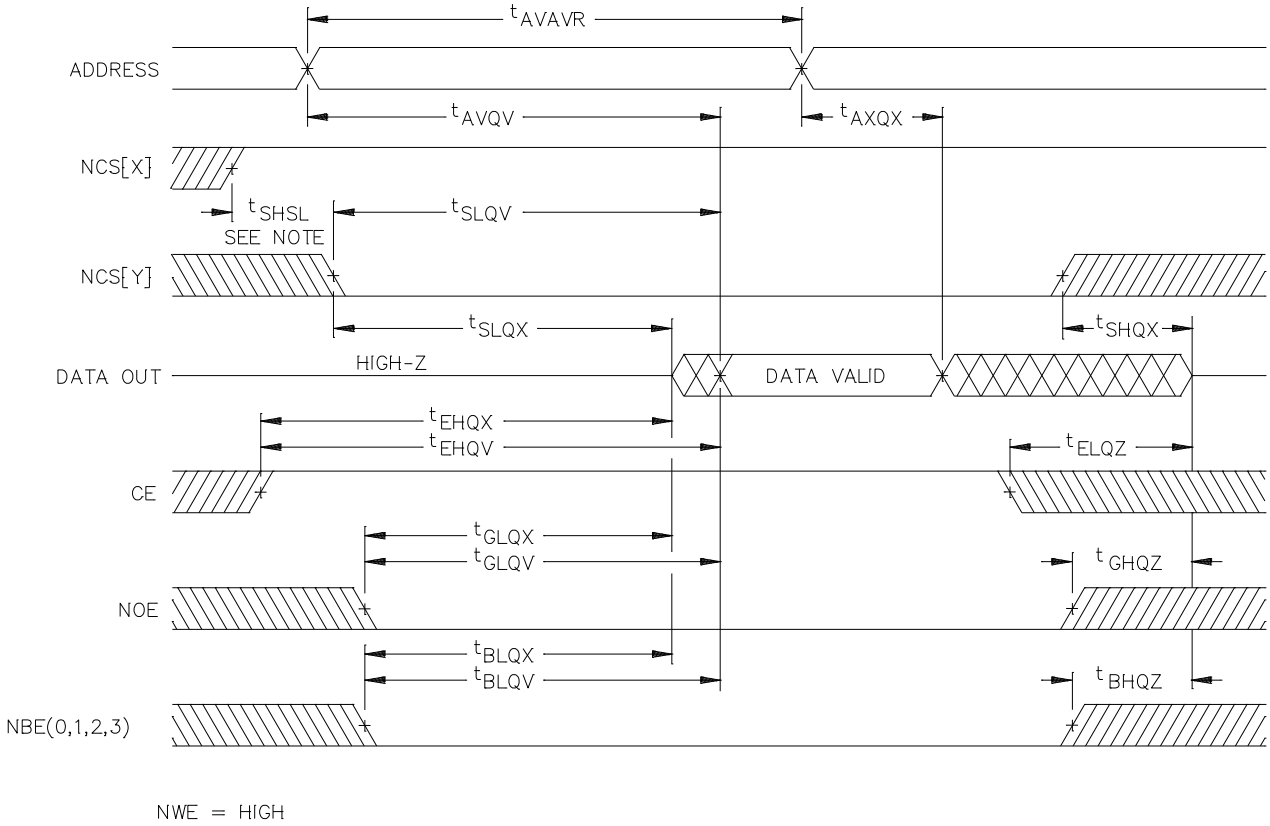


1. All input rise and fall times = 1 ns between the 90% and 10% levels
2. Timing parameter reference voltage level.
3. ss: Low-Z V_{OH} and V_{OL} steady state output voltage.
4. High-Z Output pin pulled to V_{LOAD} by output load circuit.

I/O type	$V_{IH}ac$	$V_{IL}ac$	V_{REF}	V_{LOAD}
3.3 V CMOS	V_{DDIO}	V_{SS}	$V_{DDIO}/2$	$V_{DDIO}/2$
2.5 V CMOS	V_{DDIO}	V_{SS}	$V_{DDIO}/2$	$V_{DDIO}/2$

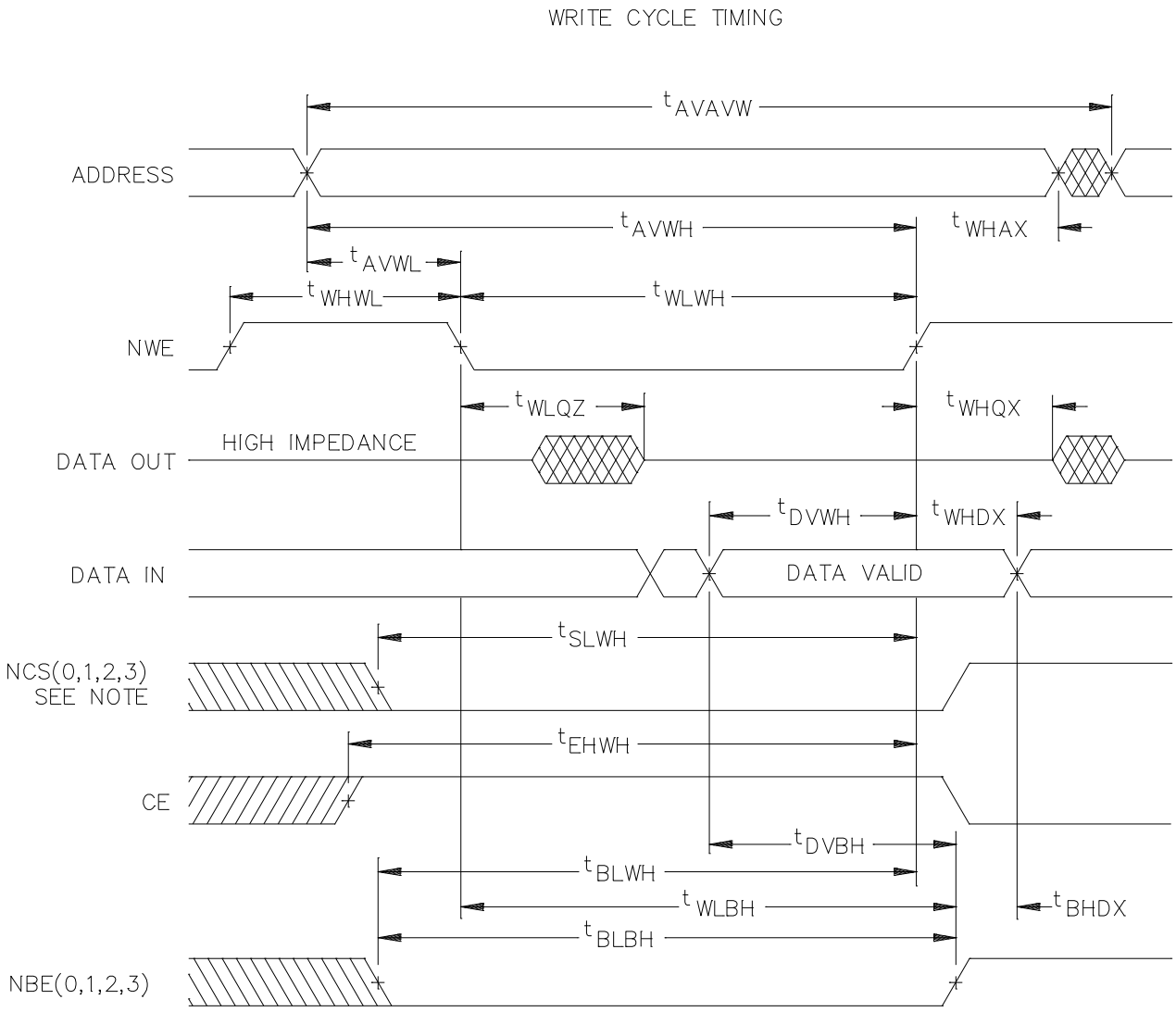
FIGURE 4. Output load circuit.

READ CYCLE TIMING



NOTE: 1. t_{SHSL} is not a tested parameter. Maintaining 4.5 ns between NCS[x] disable and NCS[y] enable will minimize contention current when switching between chip selects.
2. NCS(0, 1, 2, 3) only one NCS can be Low at a time, others must be High.

FIGURE 5. Timing waveforms.



NOTE: For an NWE controlled write NCS must be Low when NWE is Low.

FIGURE 5. Timing waveforms - Continued.

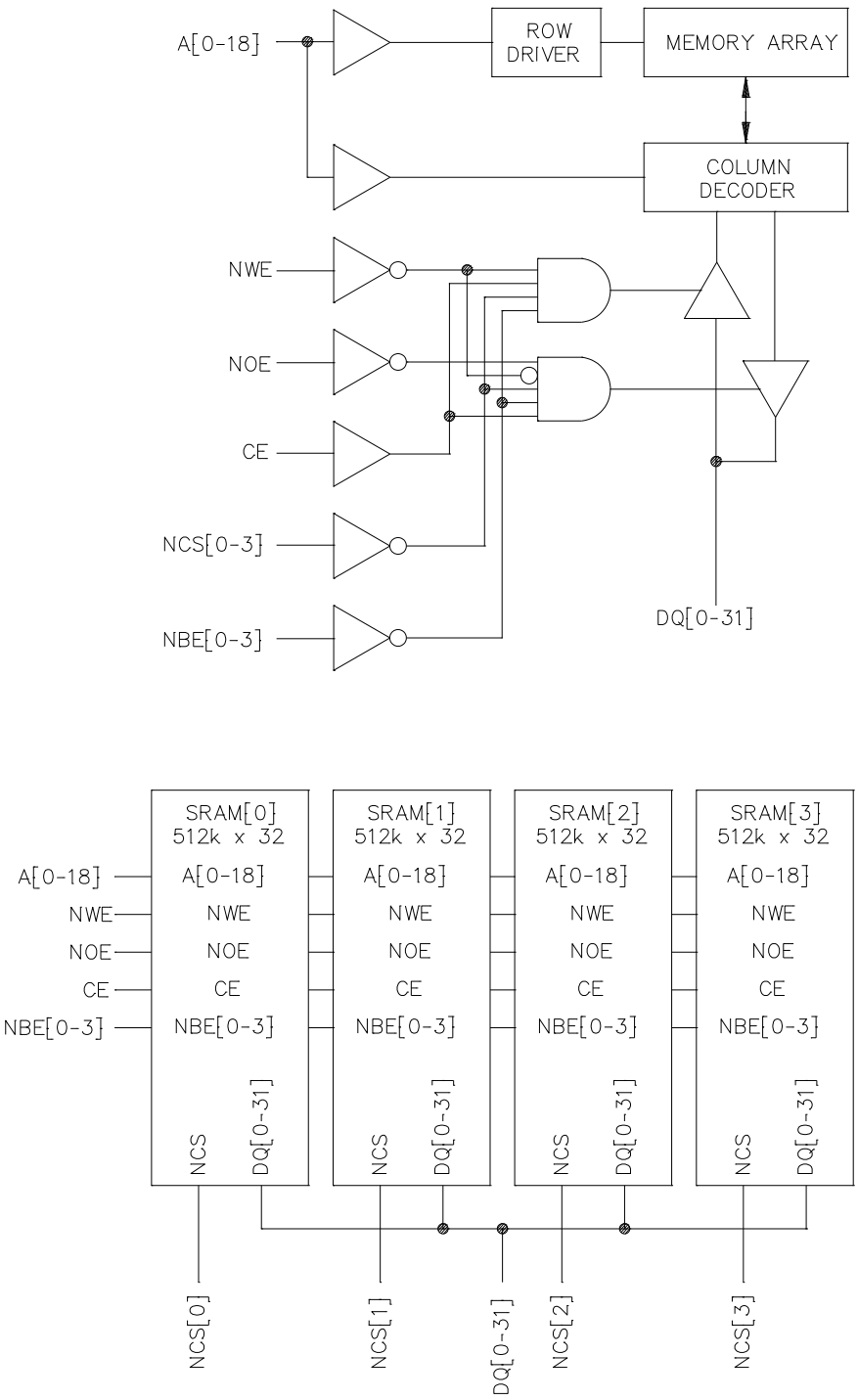


FIGURE 6. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. Capacitors are added to the package after mechanical screening.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device class Q shall be done per approved QM plan and include:
   (1) Internal visual, TM 2010 condition A
   (2) X-ray (top view only)
   (3) PIND
   (4) Serialization
   (5) 240-hour dynamic burn-in, delta, read and record (in place of standard class Q burn-in)
   (6) Static Burn-in, delta, read and record

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in Table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_A, C_{NCS}, C_{NOE}, C_{CE}, C_{NWE}, and C_D) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
2	Static burn-in I and II (method 1015)	Required	Required
3	Same as line 1	1*, 7*, 9 Δ	1*, 7*, 9 Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1*, 7*, 9 Δ	1*, 7*, 9 Δ
6	Final electrical parameters	1*,2,3,7*,8A, 8B,9,10,11	1*,2,3,7*,8A, 8B,9,10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10,11	1,2,3,4**,7,8A, 8B,9,10,11
8	Group C end-point electrical parameters	1,2,3,7,8A,8B, 9,10,11	1,2,3,7,8A,8B, 9,10,11 Δ
9	Group D end-point electrical parameters	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.
7/ See 4.4.1d.

Table IIB. Delta limits. 1/ 2/

Symbol	Parameter	Delta ±
I_{DDSB}	Core Standby Current	10% of referenced spec or 400µA
I_{DDDSB}	I/O Standby Current	10% of referenced spec or 400µA
I_{DR1}	Core Data Retention Current	10% of referenced spec or 200µA
I_{DR2}	I/O Data Retention Current	10% of referenced spec or 200µA
I_{ILK}	Input Current	10% of referenced spec or 2.0µA
I_{OLK}	Output Leakage Current	10% of referenced spec or 4.0µA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.
2/ Parameter shifts for leakage parameters are calculated at -55°C only.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in Table IIA herein. Sample size for Group D Subgroups 3 through 5 shall be 5(0) with acceptance on zero failures.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in Table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ± 5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.6 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.6 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60º to the normal, inclusive (i.e. 0º ≤ angle ≤ 60º). No shadowing of the ion beam due to fixturing or package related effects are allowed.
b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.
c. The flux shall be between 10^2 and 10^6 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
d. The particle range shall be ≥ 20 microns in silicon.
e. The test temperature shall be +25°C for upset and the maximum rated operating temperature +125ºC for latchup.
f. Bias conditions shall be defined by the manufacturer for latchup measurements.
g. For SEP test limits, see table IB herein.

4.4.4.5 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in Table IIA herein at T_A = +25°C ± 5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Signal definitions.

A (0-18)	Address input signals. Used to select a particular 32 bit word within the memory array.
DQ (0-31)	Bi-directional data signals. These function as data outputs during a read operation and as data inputs during a write operation.
NCS(0-3)	Negative Chip Select input signal. The 2Mx32 SRAM consists of four 512Kx32 SRAMs. Each 512Kx32 SRAM is controlled by a separate NCS. Setting to a low level allows normal read or write operation of the selected SRAM. Only one NCS shall be low at a time. When at a high level, it sets the selected SRAMs to a deselected condition and holds the data output drivers in a high impedance state.
NWE	Negative Write Enable input signal. Setting to a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level it allows normal read operation.
NOE	Negative Output Enable input signal. Setting to a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS, NBE, CE and NWE. If this signal is not used, it must be connected to VSS.
CE	Chip Enable input signal. When set to a high level, the SRAM is in normal read or write operation. When at a low level, it defaults the SRAM to a pre-charge condition and holds the data output drivers in a high impedance state. If the CE signal is not used, it must be connected to VDDD.
NBE (0-3)	Not Byte Enable input signal. When set to a low level, enables a read or write operation on a specific byte within the 32 bit (4 byte) word. When at a high level, the write operation of a specific byte is disabled and during a read operation the 8 data outputs of the specific byte are held in a high impedance state.
V_{SS}	Ground
V_{DD}	SRAM Core operating voltage (typical 1.8V)
V_{DDD}	I/O Operating voltage (typical 3.3V)
Cathode and Anode	These signals are used for manufacturing test only. They shall be connected to VSS.

6.8 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latchup (SEL).

APPENDIX A

Appendix A forms a part of SMD 5962-10232

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March left - right.

Step 1. Increment address from minimum to maximum writing each address with alternating data pattern (x55).
Step 2. Increment address from minimum to maximum while performing 2a and 2b
Step 2a. Read and verify an address.
Step 2b. Write the address with complement data.
Step 3. Decrement address from maximum to minimum while performing 3a, 3b, 3c, 3d
Step 3a. Read and verify an address.
Step 3b. Write the address with complement data.
Step 3c. Read and verify the address.
Step 3d. Write the address with complement data.
Step 4. Decrement address from maximum to minimum while performing 4a and 4b
Step 4a. Read and verify the address
Step 4b. Write the address with complement data
Step 5. Decrement address from maximum to minimum while performing 5a, 5b, 5c, and 5d
Step 5a. Read and verify the address
Step 5b. Write the address with complement data
Step 5c. Read and verify the address
Step 5d. Write the address with complement data
Step 6. Decrement address from maximum to minimum while performing 6a
Step 6a. Read and verify the address

FUNCTIONAL ALGORITHMS

A.3.3 Algorithm C (pattern 3).

A.3.3.1 Solids.

Step1. Write x00 data pattern to all addresses from minimum to maximum.
Step 2. Read and verify x00 data pattern at all addresses.
Step 3. Write xFF data pattern to all addresses from minimum to maximum.
Step 4. Read and verify xFF data pattern at all addresses.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Control signals functional Verification.

Each test performed independently.
NOE Functional test: Read with NOE = V_{IH} and confirm high-Z outputs
NCS Functional test: Read with NCS = V_{IH} and verify high-Z outputs

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-12-04

Approved sources of supply for SMD 5962-10232 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H1023201QXC	34168	HXSR06432-DWH
5962H1023201VXC	34168	HXSR06432-DVH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell Inc. 12001 State Highway 55 Plymouth, MN 55441