HXSR01608
2M x 8 STATIC RAM

The monolithic 2M x 8 Radiation Hardened Static RAM is a high performance 2,097,152 word x 8-bit static random access memory, fabricated with Honeywell's 150nm silicon-on-insulator CMOS (S150) technology. It is designed for use in low voltage systems operating in radiation environments. The SRAM operates over the full military temperature range and requires a core supply voltage of 1.8V and supports I/O supply voltages of 2.5V and 3.3V.

Honeywell's S150 technology is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques. There is no internal ECC implemented.

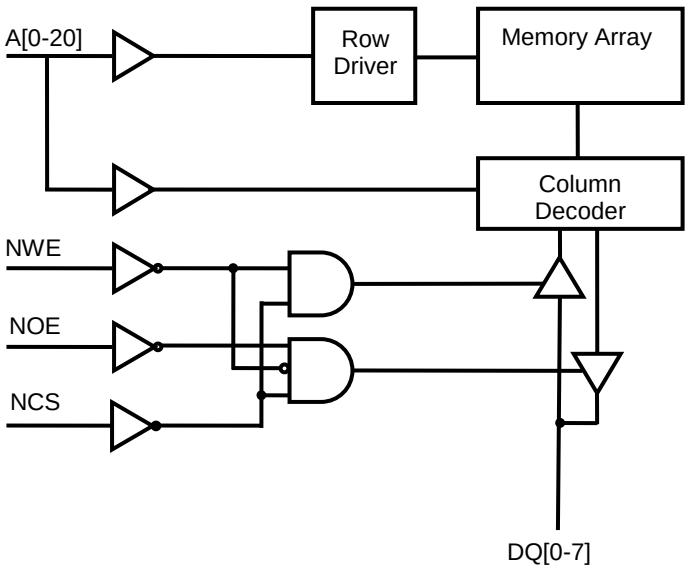
It is a low power process with a minimum drawn feature size of 150nm. This delivers high speed typical READ cycle time of 13ns, WRITE cycle time of 9ns and low power consumption of 150mW at 40MHz.

The memory cell is single event upset hardened, while four layer metal power busing and small collection volumes of SOI provides superior single event effect and dose rate hardening.

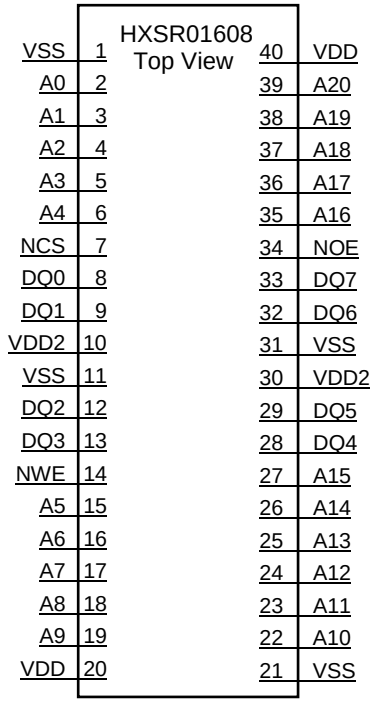
FEATURES

- Fabricated on S150 Silicon On Insulator (SOI) CMOS
- 150nm Process (Leff = 110nm)
- High Speed
  9ns Typical Write Cycle
  13ns Typical Read Cycle
- Asynchronous Operation
- CMOS Compatible I/O
- Total Dose $3x10^{5}$ and $1x10^{6}$ rad(Si)
- Soft Error Rate
  Heavy Ion $1x10^{-12}$ upsets/bit-day
  Proton $2x10^{-12}$ upsets/bit-day
- Neutron Irradiation $1x10^{14}$ n/cm^2
- Dose Rate Upset
  $1x10^{10}$ rad(Si)/s
- Dose Rate Survivability
  $1x10^{12}$ rad(Si)/s
- Latchup Immune
- Core Operating Voltage
  1.8V
- I/O Voltages
  2.5V or 3.3V
- Operating Temperature Range
  -55°C to +125°C
- 40-Lead Ceramic Flat Pack Package

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



40 LEAD FLAT PACK PINOUT



PIN NAME DEFINITIONS

Pin Name	Timing Symbol	Definition
A[0-20]	A	Address input pins. Selects a particular 8-bit word within the memory array.
DQ[0-7]	D Q	Bi-directional data I/O pins. Data inputs (D) during a write operation. Data outputs (Q) during a read operation.
NCS	S	Negative chip select. Low allows normal read or write operation. High puts the SRAM into a deselected condition and holds the data output drivers in a high impedance (High-Z) state. If not used, it must be connected to VSS.
NWE	W	Negative write enable. Low activates a write operation and holds the data output drivers in a high impedance (High-Z) state. High allows normal read operation.
NOE	G	Negative output enable. High holds the data output drivers in a high impedance (High-Z) state. Low the data output driver state is defined by NCS and NWE. If not used, it must be connected to VSS.
VDD		Power input. Supplies power for the SRAM core.
VDD2		Power input. Supplies power for the I/O.
VSS		Ground

TRUTH TABLE

NCS	NWE	NOE	MODE	DQ Mode
H	X	X	Deselect	High-Z
L	H	H	Read Standby	High-Z
L	H	L	Read	DATA OUT
L	L	X	Write	DATA IN

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Ratings		Unit
		Min	Max	
VDD2	Positive Supply Voltage (I/O) Referenced to VSS	-0.5	4.4	V
VDD	Positive Supply Voltage (core) Referenced to VSS	-0.5	2.4	V
VIO	Voltage on Any Input or Output Pin Referenced to VSS	-0.5	VDD2 + 0.5	V
IOUT	Average Output Current		15	mA
TSTORE	Storage Temperature	-65	150	°C
TSOLDER (2)	Soldering Temperature		270	°C
PD (3)	Package Power Dissipation		2.5	W
PJC	Package Thermal Resistance (Junction to Case)		2.0	°C/W
VPROT	Electrostatic Discharge Protection Voltage (Human Body Model)	2000		V
TJ	Junction Temperature		175	°C

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Maximum soldering temperature can be maintained for no more than 5 seconds.
(3) IDDSB power + IDDOP power + Output driver power due to external loading must not exceed this specification.

RECOMMENDED OPERATING CONDITIONS (1)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
VDD2	Positive Supply Voltage (3.3V I/O) Referenced to VSS	3.0	3.3	3.6	V
	Positive Supply Voltage (2.5V I/O) Referenced to VSS	2.3	2.5	2.7	V
VDD	Positive Supply Voltage (core) Referenced to VSS	1.65	1.80	1.95	V
TC	Case Temperature	-55	25	125	°C
VIO	Voltage on Any Input or Output Pin Referenced to VSS	-0.3		VDD2 + 0.3	V
TRAMP	VDD and VDD2 Power Supply Ramp Rate			1	s
TPD (2)(3)	VDD Power Down Time	5			ms

(1) Specifications listed in datasheet apply when operated under the Recommended Operating Conditions unless otherwise specified.
(2) Guaranteed, but not tested.
(3) Power Supplies must be at the VSS level for the Power Down Time (TPD) before being turned back on.

RADIATION HARDNESS RATINGS (1)

Symbol	Parameter	Environment Conditions	Limits	Unit
TID	Total Ionizing Dose		$1x10^6$ $3x10^5$	rad(Si)
DRU	Transient Dose Rate Upset	Pulse width ≤20ns	$1x10^{10}$	rad(Si)/s
DRS	Transient Dose Rate Survivability	Pulse width ≤20ns	$1x10^{12}$	rad(Si)/s
SER (2)	Projected Soft Error Rate Heavy Ion Proton	Geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield	 $1x10^{-12}$ $2x10^{-12}$	 upsets/bit-day upsets/bit-day
	Neutron Irradiation Damage	1 MeV equivalent energy	$1x10^{14}$	n/cm^2

(1) Device will not latchup when exposed to any of the specified radiation environments.
(2) Calculated using CREME96.

RADIATION CHARACTERISTICS

Total Ionizing Dose Radiation
The S150 SRAM radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Single Event Soft Error Rate
Special process, memory cell, circuit and layout design considerations are included in the SRAM to minimize the impact of heavy ion and proton radiation and achieve small projected SER. These techniques sufficiently harden the SRAM such that cell redundancy and scrubbing are not required to achieve the projected SER.

Transient Dose Rate Ionizing Radiation
Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. This allows the SRAM to be capable of writing, reading, and retaining stored data during and after exposure to a transient dose rate ionizing radiation pulse, up to the DRU specification. The SRAM will also meet functional and timing specifications after exposure to a transient dose rate ionizing radiation pulse up to the DRS specification.

Neutron Irradiation Damage
SOI CMOS is inherently tolerant to damage from neutron irradiation. The SRAM meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup
The SRAM will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

PIN CAPACITANCE (1)

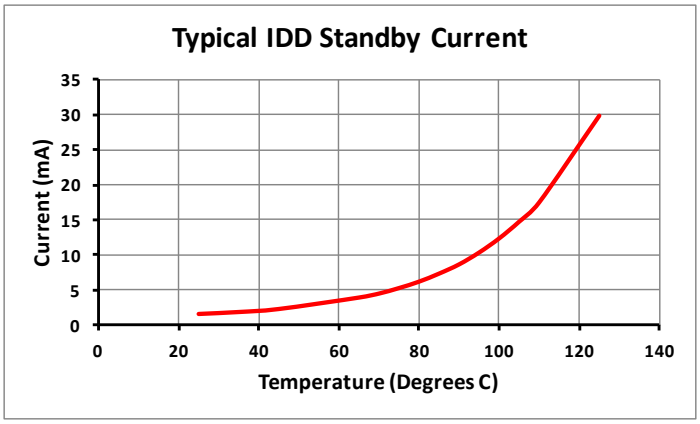
Symbol	Parameter	Max	Unit
CA	Address Pin Capacitance	7	pF
CNOE	NOE Pin Capacitance	17	pF
CNWE	NWE Pin Capacitance	17	pF
CNCS	NCS Pin Capacitance	20	pF
CDQ	Data I/O Pin Capacitance	7	pF

(1) Maximum capacitance is verified as part of initial qualification only.

POWER PIN ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		Max		Unit
				VDD	VDD2	
IDDSB (1)	Static Supply Current	VIH = VDD2, VIL = VSS, DQ = High-Z	TA=25°C, pre-TID	5	0.3	mA
				30	0.3	mA
IDDOPW (2)(3)	Dynamic Supply Current Selected, Write	VIH = VDD2, VIL = VSS, DQ = High-Z	1MHz	2	0.2	mA
			2MHz	4	0.4	mA
			10MHz	20	2	mA
			25MHz	50	5	mA
			40MHz	80	8	mA
IDDOPR (2)(3)	Dynamic Supply Current Selected, Read	VIH = VDD2, VIL = VSS, DQ = High-Z	1MHz	1	0.2	mA
			2MHz	2	0.4	mA
			10MHz	10	2	mA
			25MHz	25	5	mA
			40MHz	40	8	mA
IDDOPD (2)(3)	Dynamic Supply Current Deselected	VIH = VDD2, VIL = VSS, DQ = High-Z	1 MHz	0.1	0.2	mA
			40MHz	2	5	mA
IDRRD	Data Retention Supply Current	VDD = 1V, VDD2 = 2V	TA=25°C, pre-TID (4)	3.3	0.2	mA
				20	0.2	mA

(1) See figure “Typical IDD Standby Current, Pre-TID” below for typical pre-TID current values. This is provided for information only.
(2) All inputs switching. DC average current.
(3) All dynamic operating mode current measurements (IDDOPx) exclude standby mode current (IDDSB).
(4) This is an estimated maximum for reference and is not a pass/fail criteria. This is provided for information only.



SIGNAL PIN ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter	Conditions	Min	Max	Unit
IIN	Input Leakage Current	VSS ≤ VIN ≤ VDD2	-5	5	uA
IOZ	Output Leakage Current	DQ = High-Z	-10	10	uA
VIL (2)	Low-Level Input Voltage			0.3 x VDD2	V
VIH (2)	High-Level Input Voltage		0.7 x VDD2		V
VOL1	Low-Level Output Voltage for 3.3V I/O	IOL = 10mA		0.4	V
VOH1	High-Level Output Voltage for 3.3V I/O	IOH = -5mA	2.7		V
VOL2 (2)	Low-Level Output Voltage for 2.5V I/O	IOL = 10mA		0.4	V
VOH2 (2)	High-Level Output Voltage for 2.5V I/O	IOH = -5mA	2.0		V

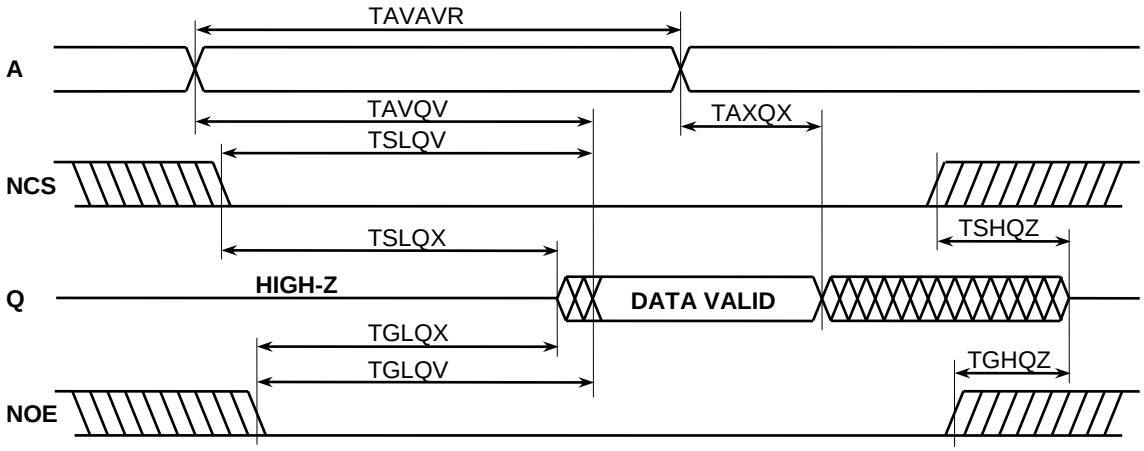
(1) Voltages referenced to VSS.
(2) Guaranteed, but not tested for 2.5V I/O.

READ CYCLE TIMING CHARACTERISTICS (1)(2)

Symbol	Parameter	Limits 2.5V I/O		Limits 3.3V I/O		Unit
		Min	Max	Min	Max	
TAVAVR	Read Cycle Time	22		20		ns
TAVQV	Address Valid to Output Valid Access Time		22		20	ns
TAXQX	Address Change to Output Invalid Time	4		4		ns
TSLQV	Chip Select to Output Valid Access Time		22		20	ns
TSLQX	Chip Select to Output Low-Z Time	0		0		ns
TSHQZ	Chip Select to Output High-Z Time		4		4	ns
TGLQV	Output Enable to Output Valid Access Time		6		6	ns
TGLQX	Output Enable to Output Low-Z Time	0		0		ns
TGHQZ	Output Enable to Output High-Z Time		4		4	ns

(1) The timing specifications are referenced to the Timing Input and Output References diagram and the Timing Reference Load Circuit diagram. IBIS models should be used to evaluate timing under application load circuits.
(2) NWE = High

READ CYCLE TIMING WAVEFORMS



WRITE CYCLE TIMING CHARACTERISTICS (1)(2)(3)

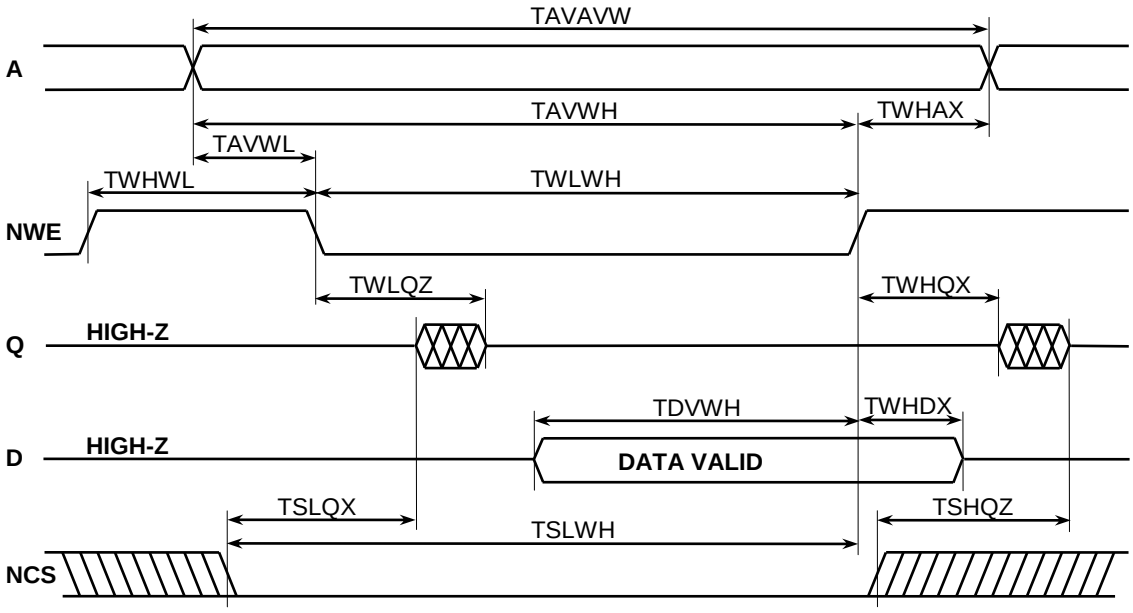
Symbol	Parameter	Limits 2.5V I/O		Limits 3.3V I/O		Unit
		Min	Max	Min	Max	
TAVAVW	Write Cycle Time	12		12		ns
TWLWH	Start of Write to End of Write Pulse Width	7		7		ns
TSLWH	Chip Select to End of Write Time	10		10		ns
TDVWH	Data Input Valid to End of Write Time	6		6		ns
TAVWH	Address Valid to End of Write Time	12		12		ns
TWHDX	Data Input Hold after End of Write Time	0		0		ns
TAVWL	Address Valid Setup to Start of Write Time	0		0		ns
TWHAX	Address Valid Hold after End of Write Time	0		0		ns
TWLQZ	Start of Write to Output High-Z Time		4		4	ns
TWHQX	End of Write to Output Low-Z Time	0		0		ns
TWHWL	End of Write to Start of Write Pulse Width	5		5		ns

(1) The timing specifications are referenced to the Timing Input and Output References diagram and the Timing Reference Load Circuit diagram. IBIS models should be used to evaluate timing under application load circuits.

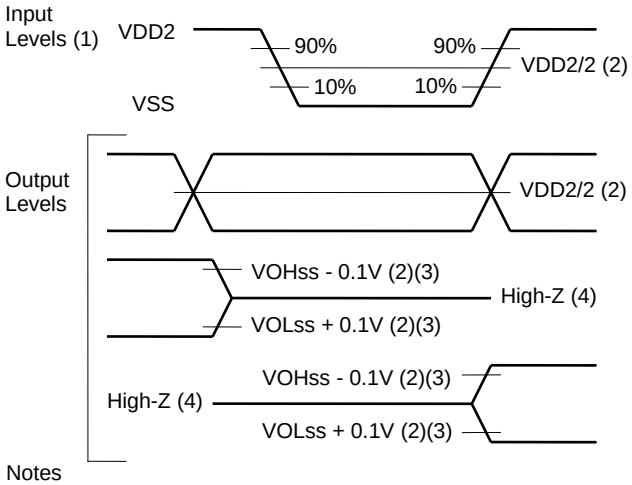
(2) For an NWE controlled write, NCS must be Low when NWE is Low.

(3) Can use NOE = High to hold Q in a High-Z state when NWE = High and NCS = Low.

WRITE CYCLE TIMING

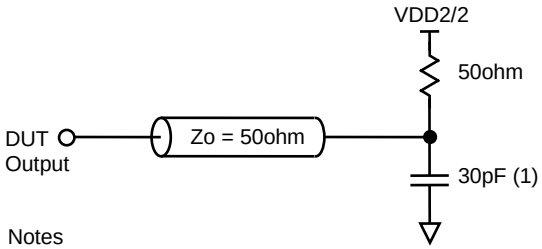


TIMING INPUT AND OUTPUT



Notes
(1) Input rise and fall times = 1ns between 90% and 10% levels.
(2) Timing parameter reference voltage level.
(3) ss: Low-Z VOH and VOL steady-state output voltage.
(4) High-Z output pin pulled to VDD2/2 by Reference Load Circuit.

TIMING REFERENCE LOAD



Notes
(1) Set to 5pF for T*QZ (Low-Z to High-Z) timing parameters.

FUNCTIONAL DESCRIPTION

SRAM Operation
SRAM operation is asynchronous. Operating modes are defined in the Truth Table. Read operations can be controlled by Address (A[0-18]) or Chip Select (NCS). Write operations can be controlled by Write Enable (NWE) or Chip Select (NCS).

Read Operation
A read operation occurs when Chip Select (NCS) is low and Write Enable (NWE) is high. The output drivers are controlled independently by the Output Enable (NOE) signal.

To control a read cycle with NCS where TSLQV is the access time, all addresses must be valid TAVQV minus TSLQV prior to the enabling NCS transition. Address transitions can occur later; however, the valid Data Output (Q) access time will then be defined by TAVQV instead of TSLQV. NCS can disable the read at any time; however, Data Output drivers will enter a High-Z state TSHQZ later.

To control a read cycle with Address where TAVQV is the access time, NCS must transition low TSLQV minus TAVQV prior to the last Address transition. The NCS transition low can occur later; however, the valid Data Output (Q) access time will then be defined by TSLQV instead of TAVQV. To perform consecutive read cycles, NCS is held continuously low, and the toggling of any Address will start a new read cycle. Any amount of toggling or skew between Address transitions is permissible; however, Data Output will not become valid until TAVQV following the last occurring Address transition. The minimum Address activated read cycle time is TAVAVR which is the time between the last Address transition of the previous cycle and the first Address transition of the next cycle. The valid Data Output from a previous cycle will remain valid until TAXQX following the first Address transition of the next cycle.

Write Operation
A write operation occurs when Write Enable (NWE) is low and Chip Select (NCS) is low. Either NWE or NCS can start the write mode and either can end the write mode, but the write operation itself is defined by the overlap of NCS low and NWE low. Both modes of control are similar, except the NCS controlled mode disables the SRAM when NCS is high between writes. NWE/NCS controls the start of write when NCS/NWE transitions low before NWE/NCS transitions low. NWE/NCS controls the end of write when NCS/NWE transitions high after NWE/NCS transitions high.

To write Data (D) into the SRAM, NWE and NCS must be held low for at least TWLWH and TSLSH respectively. Any amount of skew between these signal transitions can be tolerated, and either one of these control signals can start or end the write operation as long as TSLWH and TWLSH are met.

Address inputs must be valid at least TAVWL/TAVSL before the start of write from an NWE/NCS transition low and TAVWH/TAVSH before the end of write from an NWE/NCS transition high and must remain valid during the write operation. Hold times for address inputs with respect to the end of write from a NWE/NCS transition high must be a minimum of TWHAX/TSHAX.

A Data Input (D) valid to the end of write time from an NWE/NCS transition high of TDVWH/TDVSH must be provided during the write operation. Hold times for Data Input with respect to the disabling NWE/NCS transition high must be at least TWHDX/TSHDX. To avoid Data Input driver contention with the SRAM output driver, the Data Input (D) must not be applied until TWLQZ/TGHQZ after the output drive (Q) is put into a High-Z condition by NWE/NOE.

Consecutive write cycles are performed by toggling at least one of the NCS or NWE control signals high for TWHWL/TSHSL. If only one of these signals is used, the other must be in its write enable state (NWE or NCS held low). The minimum NWE/NCS write cycle time is TAVAVW/TAVAVS.

Signal Integrity

As a general design practice, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns. This is especially important in a selected and enabled state. When the device is selected and enabled, the last transitioning input for the desired operation must have good signal integrity to maintain valid operation. The transitioning inputs that bring the device into and out of a selected and enabled state must also have good signal integrity to maintain valid operation. When the device is deselected and/or disabled, inputs can have poor signal integrity and even float as long as the inputs that are defining the deselected and/or disabled state stay within valid VIL and VIH voltage levels. However, floating inputs for an extended period of time is not recommended.

RELIABILITY

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

SCREENING AND CONFORMANCE INSPECTION

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

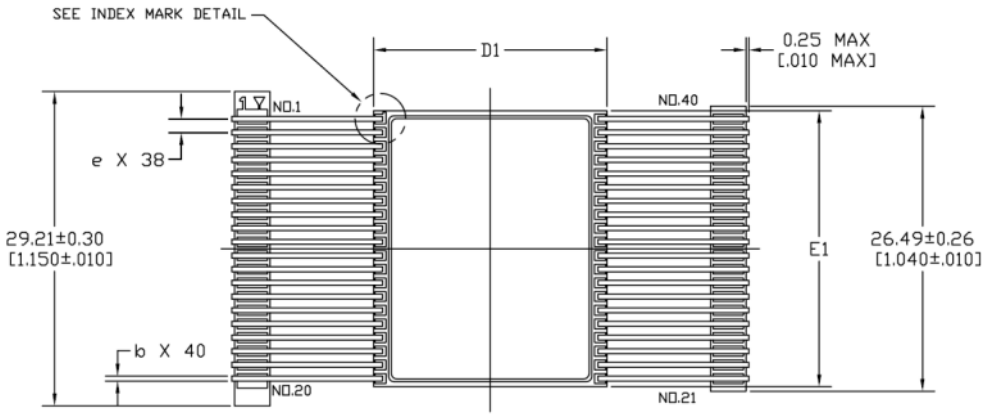
Conformance Summary

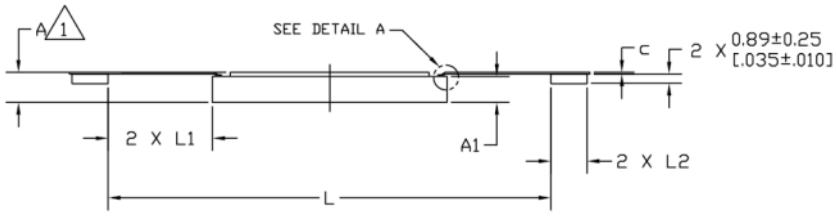
Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests - 1000 hours at 125C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

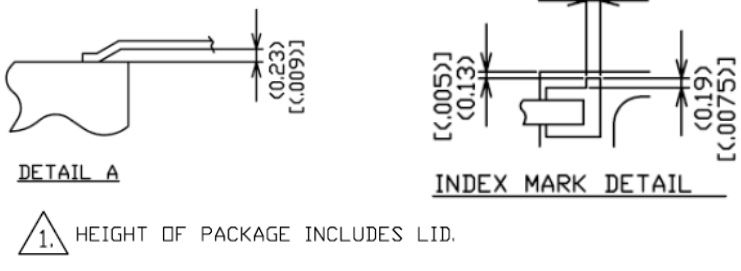
PACKAGE FEATURES

Feature	Description
Designation	A
Type	40-lead flat pack
Body Construct	multi-layer ceramic (Al_2O_3)
Power Planes	Yes
Lid Construct	Kovar
Lid Electrical Connection	VSS
Body Dimensions (nominal)	21.67 x 25.65 x 2.87 mm
Weight	6.5g

PACKAGE OUTLINE







1. HEIGHT OF PACKAGE INCLUDES LID.

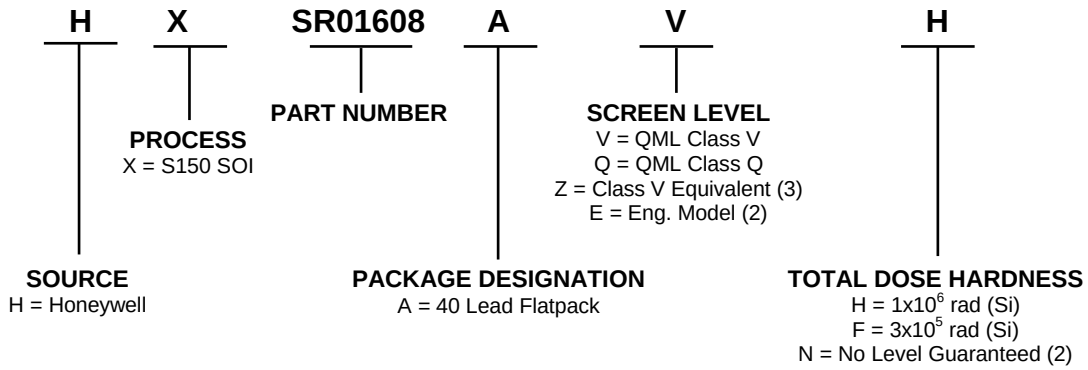
SYMBOL	COMMON DIMENSIONS (MILLIMETERS)			COMMON DIMENSIONS (INCHES)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.62	2.87	3.13	.102	.112	.122
A1	2.17	2.41	2.65	.086	.095	.104
b	0.41	0.46	0.51	.016	.018	.020
c	0.10	0.15	0.20	.004	.006	.008
D1	21.47	21.67	21.87	.845	.853	.891
e	1.14	1.27	1.40	.045	.050	.055
E1	25.45	25.65	25.85	1.002	1.010	1.018
L	---	40.89	---	---	1.610	---
L1	9.25	9.61	---	.364	.379	---
L2	3.10	3.30	3.50	.122	.130	.138

HXSR01608

ORDERING INFORMATION (1)

Standard Microcircuit Drawing

The HXSR01608 SRAM can be ordered under the SMD drawing 5692-08202.



(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 or 1-800-323-8295 for further information.
(2) Engineering Model Description: Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation guaranteed.
(3) These receive the Class V screening and QCI is included. Customer must specify QCI requirements.

QCI TESTING (1)(2)

Classification	QCI Testing
QML V Equivalent	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

Notes:
(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell QM Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

FIND OUT MORE

For more information about Honeywell's family of radiation hardened integrated circuit products and services, visit www.honeywellmicroelectronics.com.

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ADS-14155 Rev. E
April2015