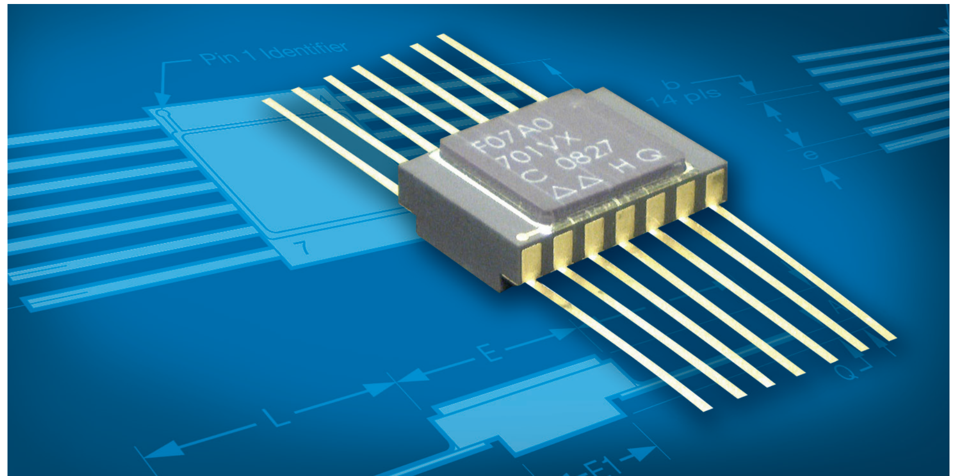
HXNAND00

Honeywell

Quad 2 Input NAND

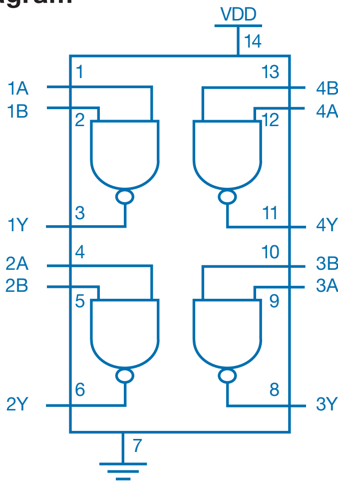
Features

- **Radiation Hardened**
  Total Dose: 300krad (Si)
- **Supply voltage:**
  3.3V
- **Quiescent current:**
  500µA
- **Max Prop Delay**
  6.6nS
- **Max Rise/Fall Time**
  4.3nS
- **Input capacitance**
  11.5pF max
- **Output resistance**
  15Ω max



The HXNAND00 is a Quad 2 input NAND which is fabricated on a radiation hardened SOI-V Silicon–On-Insulator (SOI) 0.35µm CMOS process with very low power consumption. The device contains Schmitt-Trigger inputs and specially designed output buffers to provide high drive. Honeywell's SOI-V technology is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques.

Functional Diagram



Truth Table

Input A	Input B	Output
L	L	H
L	H	H
H	L	H
H	H	L

Signal Definitions

Pin	Symbol	Type
1	1A	IN
2	1B	IN
3	1Y	OUT
4	2A	IN
5	2B	IN
6	2Y	OUT
7	GND	GND
8	3Y	OUT
9	3A	IN
10	3B	IN
11	4Y	OUT
12	4A	IN
13	4B	IN
14	VDD	PWR

PRODUCTION - Release - 21 Jul 2014 02:49:45 MST - Printed on 21 Jul 2014

Radiation Characteristics

Total Ionizing Dose Radiation

The device radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Transient Dose Rate Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. The device will maintain basic functional operation during exposure to a pulse up to the DRU specification. The device will meet functional, timing and parametric specifications after exposure to a pulse up to the DRS specification.

Neutron Irradiation Damage

SOI CMOS is inherently tolerant to damage from neutron irradiation. The device meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup

The device will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

Radiation-Hardness Ratings (1)

Parameter	Symbol	Environment Conditions	Limits	Units
Total Dose	TID		300	krad(Si)
Transient Dose Rate Upset	DRU	Pulse width ≤ 20ns	$1x10^{9}$	rad(Si)/s
Dose Rate Survivability	DRS	Pulse width ≤ 20ns	$1\ x10^{12}$	rad(Si)/s
Neutron Irradiation Damage		1MeV equivalent energy	$1\ x10^{14}$	N/cm^2

(1) Device will not latch up due to any of the specified radiation exposure conditions.

Absolute Maximum Ratings (1)(2)

Parameter	Symbol	Rating Min	Rating Max	Units
Supply Voltage	VDD	-0.5	4.6	V
DC Input Voltage	V_{IN}	-0.5	VDD+0.5	V
DC Output Voltage	V_{OUT}	-0.5	VDD+0.5	V
Electrostatic Discharge Protection Voltage (Human Body Model)	V_{PROT}		2000	V
Storage Temperature	T_{STORE}	-65	150	°C
Soldering Temperature (4)	T_{SOLDER}		300	°C
Maximum Junction Temperature	T_J		175	°C
Package Thermal Resistance (Junction-to-Case)	$Theta_{JC}$		7.4	°C/W
Input Diode Clamp Current	I_{IK}	-42	42	mA
Output Short Circuit Current (3)	I_{OS}	-450	680	mA
DC Output Current, Per Pin	I_O	-50	50	mA
Continuous Current Per Output Pin		-31.5	31.5	mA

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to Ground.
(3) One output shorted at a time for a maximum of 1 second.
(4) Maximum soldering temperature can be maintained for no more than 5 seconds.

Recommended Operating Conditions (1)(2)

Parameter	Symbol	Rating Min	Rating Max	Units
Supply Voltage	VDD	3.0	3.6	V
Voltage on any pin (excludes power and ground)	V_{PIN}	-0.3	VDD+0.3	V
Operating Temperature	T_{CASE}	-55	125	°C

(1) Voltage referenced to Ground.
(2) Specifications listed in datasheet apply when used under the Recommended Operating Conditions unless otherwise specified.

Capacitance (1)

Parameter	Symbol	Rating Min	Rating Max	Units
Input Capacitance	C_I		11.5	pF
Output Capacitance	C_O		23	pF

(1) Guaranteed but not tested.

DC Electrical Characteristics (1)

Parameter	Symbol	Rating Min	Rating Max	Units	Conditions
Quiescent Supply Current	IDD		500	uA	
Input Leakage Low	I_{IL}	-1	1	uA	0V ≤ VIN ≤ VDD
Input Leakage High	I_{IH}	-1	1	uA	0V ≤ VIN ≤ VDD
Positive-going Threshold Voltage	V_{T+}		VDD*0.7	V	
Negative-going Threshold Voltage	V_{T-}	VDD*0.3		V	
Hysteresis	V_{HYST}	0.25		V	
Low-Level Output Voltage	V_{OL}		0.3	V	I_O = 100uA, VDD=3.0V
			0.6	V	I_O = 12mA, VDD=3.0V
			0.8	V	I_O = 24mA, VDD=3.0V
High-Level Output Voltage	V_{OH}	VDD-0.3		V	I_O = -100uA, VDD=3.0V
		VDD-0.65		V	I_O = -12mA, VDD=3.0V
		VDD-0.75		V	I_O = -18mA, VDD=3.0V
		VDD-1.0		V	I_O = -24mA, VDD=3.0V
Output Impedance (4)	R_{OUT}	5	15	ohms	
Dynamic supply current (2)(3)	IDDOP1		+10	mA	Clock = 0.5 MHz, Data = 1 Mbps
	IDDOP2		+38	mA	Clock = 5 MHz, Data = 10 Mbps
	IDDOP3		+113	mA	Clock = 25 MHz, Data = 50 Mbps
	IDDOP4		+209	mA	Clock = 50 MHz, Data = 100 Mbps

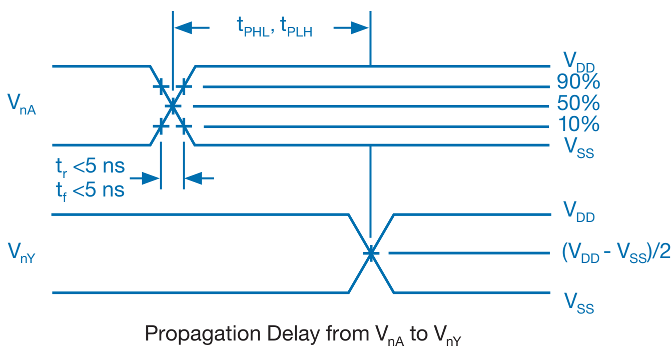
(1) Voltage referenced to Ground.
(2) VDD = 3.6 V, all outputs toggling once per cycle and all 8- inputs connected together. Load = 85 pF.
(3) Mbps reflects a data rate (i.e. data changes at time t0 for the entire cycle) and MHz reflects a clock rate (i.e. two transitions per cycle). Therefore, the clock rate will be half of the data rate.
(4) Guaranteed but not tested.

AC Timing Characteristics

Parameter	Symbol	Rating Min	Rating Max	Units
Propagation Delay	T_{PHL}, T_{PLH}	1.75	6.6	ns
Skew (1)(2)	T_{SK}		1.5	ns
Output Rise Time (1)	T_R		4.3	ns
Output Fall Time (1)	T_F		3.7	ns

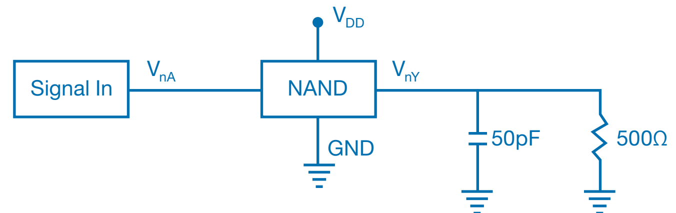
(1) Guaranteed but not tested.
(2) Skew between the propagation delays of any two outputs switching in the same direction.

Timing Diagram



Propagation Delay from V_{nA} to V_{nY}

Circuit for Switching Time



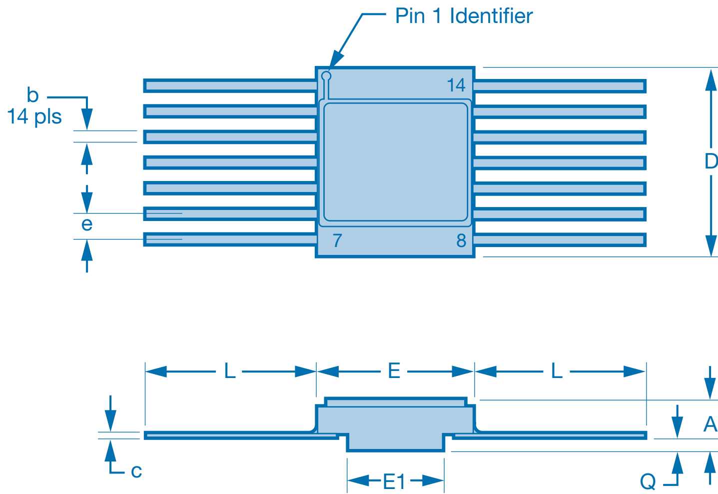
The circuit diagram is for reference only.

Signal Integrity

As a general design practice, for digital input signals, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns.

Floating inputs for an extended period of time is not recommended.

Package Definition



Dimensions

Symbol	Inches Min	Inches Max	Millimeters Min	Millimeters Max
A	.101	.125	2.57	3.18
b	.015	.019	0.38	0.48
c	.004	.007	0.11	0.18
D	.333	.347	8.46	8.82
e	.045	.055	1.14	1.40
E	.250	.261	6.33	6.63
E1	.170	.182	4.30	4.60
L	.340	.380	8.64	9.65
Q	.022	.032	0.56	0.82

Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

Screening and Conformance Inspection

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Conformance Summary

Group	Tests
Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

Ordering Information (1)

Standard Microcircuit Drawing

The HXNAND00 can be ordered under the SMD drawing 5962-07A07.

H	X	NAND00	X	V	F
Source H = Honeywell	**Process** X = SOI	**Part Number**	**Package Designation** X = 14 Pin Flatpack	**Screen Level** V = QML V W= QML Q+ E = Eng. Model (2)	**Total Dose Hardness** F = $3x10^5$ rad (Si) N = No Level Guaranteed (2)

(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 for further information.
(2) Engineering Model Description: Engineering Model suffix for Screening Level and Total Dose Hardness is "EN". Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation hardness guaranteed.

QCI Testing (1)

Classification	QCI Testing
QML Q+	No lot specific testing performed. (2)
QML V	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell QM Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

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Find out more

For more information about Honeywell's family of radiation hardened integrated circuit products and services, visit www.honeywellmicroelectronics.com/.

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ADS-14200 rev. A
June 2014
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