Honeywell

HX5SA Structured Array Platform S150 (150nm) ASICs

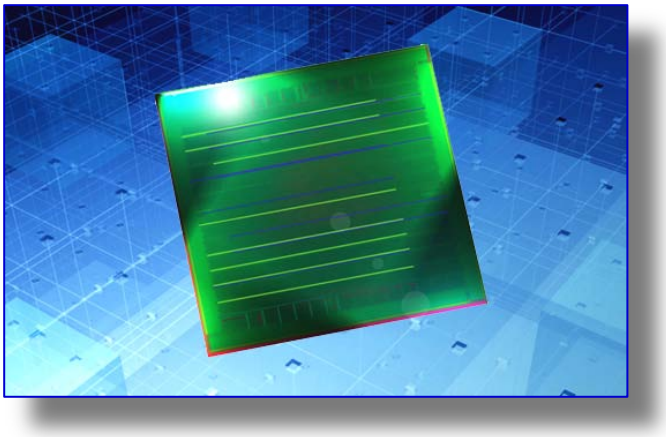
GENERAL DESCRIPTION

The Honeywell HX5SA structured array platform provides an alternative design implementation to high-end FPGAs or standard cell ASICs. By starting with a fixed array of cells and optimizing the interconnect layers for each design, the HX5SA provides high integration and high performance with short lead times and cost effectiveness. This minimizes design-to-production cycle time while enabling logic designers to receive the cost and performance advantages of an ASIC implementation with minimum design resources, cost, and risk.

The HX5SA capability initially includes a single array option, but has the capability to support additional array sizes and product features. The initial array in the family, HX5SA10, provides up to 4.5M usable gates, up to 2Mb of SRAM and is available in a 783 pin Ceramic Land Grid Array (CLGA) package.

The HX5SA Platform ASICs are manufactured on the Honeywell S150 150nm Silicon On Insulator (SOI) CMOS technology using a cell-based library and advanced ASIC design methodology. The design and manufacturing flow supports ASIC development from RTL through delivery of tested ASICs. The S150 technology is designed to withstand extremely high levels of Total Dose Radiation and the HX5SA ASIC library Flip-flops and SRAM cells are designed for low static and dynamic Soft Error Rate (SER).

The ASIC development methodology that supports these complex ASICs is based on the Synopsys toolset. This robust design flow supports flexible design handoffs with multiple entry points including specification, RTL, or synthesized gate level netlist.



Design For Test (DFT) is an integral part of this design flow.

Each HX5SA design is based on a proven ASIC library of standard logic elements, and configurable I/O cells. Macro cells such as Phase Lock Loops (PLL) and embedded dual port SRAMs are available. Designers can choose from a wide variety of I/O types. In addition to conventional LVCMOS interface levels, the HX5SA also supports PCI, LVDS, SSTL and LVPECL signaling levels. HX5SA supports 1.8V, 2.5V, and 3.3V I/O.

Customization of each design is accomplished by programming interconnect layers to minimize design time while providing high system performance and high routability.

This family is available with Honeywell's high reliability screening procedures and consistent with MIL-PRF-38535 QML Class Q and V requirements.

HX5SA10 FEATURES

- Fabricated on 150nm Silicon On Insulator (SOI) CMOS
- Total Dose Hardness: > $1x10^6$ rad (Si) available
- Ultra-low Soft Error Rate (SER)
- No Latch-up
- Low Power
  - 17 nW/Gate/MHz (1.8V)
- 49 Dual-Port SRAMs
- 4 PLLs (50MHz to 1.2GHz)
- Configurable I/O Options:
  - 1.8V/2.5V/3.3V CMOS
  - Cold spare
  - PCI
  - 2.5V, 3.3V LVDS
  - 1.8V/2.5V/3.3V SSTL
- VDSM ASIC Design Methodology based on Synopsys tool set
- Package Signal I/O count:
  - 512 configurable I/O
- Operating Voltages
  - 1.8 V ± 0.15V Core
  - 1.8V, 2.5V and 3.3V I/O
- Operating Range is -55°C to +125°C case temperature

TECHNICAL DESCRIPTION

S150 SOI CMOS Description

The Honeywell technical approach for development of HX5SA ASICs utilizes our state-of-the-art 150-nanometer SOI CMOS (S150) technology. SOI CMOS offers advantages for high-performance applications not attainable in standard bulk CMOS for radiation hardened applications. SOI devices are fabricated in a thin film of silicon on top of a buried oxide insulator on top of a standard silicon wafer. SOI has a proven history of resistance to SEU and immunity to latch-up. These advantages simplify design steps, improve density and reduce a variety of parasitic capacitances.

Reduced Power Consumption

- SOI technology offers lower capacitance than bulk CMOS of the same feature size resulting in lower power reduction
- 1.8V core operating voltage
- 1.8V, 2.5V, 3.3V I/O operating voltage options

HX5SA Technical Parameters

HX5SA Characteristics	Value
Layers of Metal	6
Minimum Geometry	0.15 µm drawn /0.11 µm L_{eff}
Operating Voltage (Core)	1.8 ± 0.15V
Operating Voltage (I/O)	1.8 ± 0.15V, 2.5 ± 0.2V, 3.3 ± 0.3V
Typical Intrinsic Delay-2 Input NAND (fan out =2)	60 ps @ 1.8V
Typical Power Dissipation, nW/Gate/MHz 20% Data, 200% Clock Activity Rate	17 @ 1.8V
Operating Temperature	-55°C to 125°C
ESD (Human Body Model)	>2000 Volts

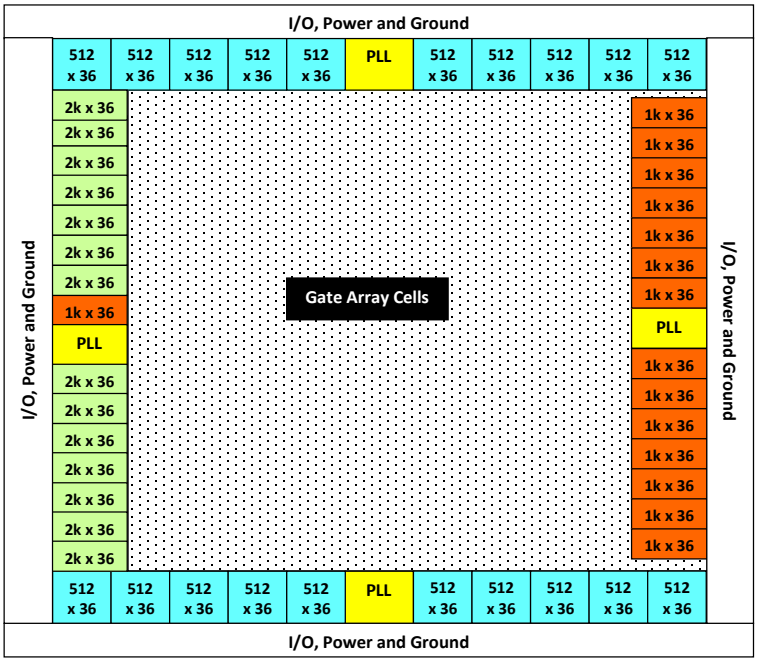
HX5SA10 Specifications

Parameter	Value
Die Size	16mm x 16mm
Usable Gates	4. 5 Million (1)
Total Number of SRAM bits	2.0 M
Number of 512x36 Dual Port SRAMs	10 each on top and bottom
Number of 1K X 36 Dual Port SRAMs	14 on right side, 1 on left side
Number of 2K X 36 Dual Port SRAMs	14 on the left side
Number of PLLs	4, one on each side
PLL Operating Frequency	50MHz to 1.2GHz
Number of I/O Signals	512
Number of VSS bond wires	136
Number of VDD (core) bond wires	64
Number of VDDIO bond wires	72

Notes:

(1) The number of routable gates is dependent on several other factors including routing densities, amount of RAM used and I/O quantity.

HX5SA10 Floor Plan Diagram (for reference, not to scale)



RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

The Structured Array will meet all stated functional and electrical specifications after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications, after an operational period of 15 years. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 KeV X-ray. Parameter correlations have been made between 10 KeV X-rays applied at dose rates of $1x10^5$ to $5x10^5$ rad(SiO_2)/min at T= 25^OC and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

Honeywell supports the highest levels of transient pulse radiation hardness. Please contact Honeywell for more information and specifications for applications requiring transient pulse hardness.

Neutron Radiation

The library elements will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The library elements are capable of meeting the specified Soft Error Rate (SER), under recommended operating conditions. The specification applies to both heavy ion and proton. This heavy ion hardness level is defined by the Adams 90% worst case cosmic ray environment for geosynchronous orbits. The HX5SA library contains several types of storage elements, including registers and embedded RAM, which provide options for single event effect mitigation.

Latchup

The array will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SOI substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p-channel and n-channel substrates are made to ensure no source/drain snapback occurs.

Radiation-Hardness Ratings

Parameter	Limits		Units	Test Conditions
Total Dose	> 1 x 10^6		Rad(Si)	VDD= 1.95 Volts, VDD3= 3.6 Volts, T_C = 25°C, Co60
Soft Error Rate (1)(3)	Standard	Asynch.		
SEUN Flip Flop	≤ 5 x 10^{-8}	≤ 5 x 10^{-8}	Upsets/bit-day (2)	VDD= 1.65 – 1.95 Volts
SEUT1 Flip Flop	≤ 2 x 10^{-10}	≤ 6 x 10^{-10}	Upsets/bit-day (2)	VDD3= 3.3 Volts
SEUT2 Flip Flop	≤ 4 x 10^{-11}	≤ 1 x 10^{-10}	Upsets/bit-day (2)	T_C = 25°C
SEUT3 Flip Flop	≤ 1 x 10^{-11}	≤ 5 x 10^{-11}	Upsets/bit-day (2)	(static or dynamic clock)
SRAM (Dual Port)	≤ 7 x 10^{-15}		Upsets/bit-day (2)	
Neutron Fluence	1x10^{14}		N/cm^2	1MeV equivalent energy

(1) There are multiple types of registers with different SER ratings to allow optimization of overall ASIC speed.
(2) Adams 90% W.C. environment GEO orbit, 100 mil shielding
(3) Standard – registers without asynchronous input pins ie dffq, dffq_scl, dffq_syr
Asynch – registers with asynchronous input pins ie dffq_ar, dffq_ash

HX5SA LIBRARY

The HX5SA library contains more than 220 standard library cells with a broad array of cell types. Many logic functions have multiple versions available to allow for trade-offs of radiation tolerance, speed, power consumption, and I/O drive strengths. Flip flops and memory cells are available in several SEU levels to support different radiation requirements.

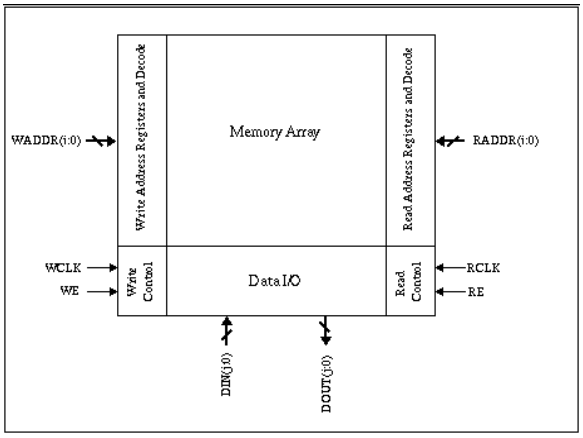
The library is designed to support use of Synopsys Module Compiler™. Module Compiler is a tool for creating high-performance, datapath-intensive modules.

Embedded SRAMs

The HX5SA family includes embedded SRAM blocks to efficiently implement large memory structures. The embedded SRAMs provide radiation hardness, high density and high performance in a dual port configuration. Access to the memory data is controlled through separate read and write ports, thus providing concurrent read and write operations. SRAMs retain data content as long as power is supplied to the memory device.

The HX5SA10 contains 49 separate embedded dual port SRAM blocks including twenty 512x36 SRAMs, fifteen 1024x36 SRAMs and fourteen 2048x36 SRAMs. The designer can implement a wider-word SRAM by connecting multiple SRAM blocks side by side, or deeper memory can be achieved by stacking multiple SRAM blocks. Typical access times are 2 to 3 ns.

The HX5SA dual port SRAMs have separate read and write ports. Dual port SRAMs are synchronous and use a write clock and a read clock to register inputs and outputs. A block diagram of an HX5SA dual port SRAM is shown in the figure below. If the read port accesses a location which is simultaneously being written to by the write port, the value on DOUT will be unknown.



Embedded Phase Lock Loops

The HX5SA10 contains 4 high performance embedded Phase Lock Loop (PLL) circuits. There is one PLL circuit in the middle of each side of the die. These circuits can be used to provide frequency synthesis, insertion delay cancellation, high-frequency clock synchronization or clock multiplication on chip. The range of the PLL operating frequency is 50MHz to 1.2GHz. The table below lists the general specifications of the PLLs.

PLL Electrical Performance Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Comment
OUTCLK frequency	fOUTCLK	50		1200	MHz	Use FS[2:0] to select OUTCLK range.
REFCLK frequency	fREFCLK	25		500	MHz	
FBKCLK frequency	fFBKCLK	25		500	MHz	
Maximum Power	Pmax			40	mW	fOUTCLK=1200MHz
Analog Power Supply Voltage	VDDA	1.65	1.8	1.95	V	
Digital Power Supply Voltage	VDD	1.65	1.8	1.95	V	
Frequency multiplication	N					Max divide ratio from OUTCLK and FBKCLK to multiply fREFCLK
VCO I (50-200 MHz)	N	1		10		FS = 000, 001
VCO II (180-630 MHz)	N	1		32		FS = 010, 011
VCO III (600-1200 MHz)	N	2		40		FS = 100, 101
Lock Time				250	us	
REFCLK						
Input rise/fall time	tr/f		0.16	0.33	ns	10 – 90 %
Jitter	Jpp			150	ps p-p	fREFCLK=500MHz
Minimum Pulse Width High		800			ps	
Minimum Pulse Width Low		800			ps	
OUTCLK						
Maximum load	CL			400	fF	
Output Jitter (Phase)	Jpp					
VCO I (50-200 MHz)	Jpp			60	ps	FS = 000, 001
VCO II (180-630 MHz)	Jpp			40	ps	FS = 010, 011
VCO III (600-1200 MHz)	Jpp			40	ps	FS = 100, 101
Output Jitter (Cycle to Cycle)	Jpp (cc)			100	ps	OUTCLK= 50 - 1200MHz

HX5SA I/O Options

Honeywell's HX5SA family I/O cells provide a wide variety of user options for interfacing to other devices in the system. The I/O cells provide buffering and drive for signals entering or leaving the device. In addition to conventional LVCMOS interface levels, the HX5SA family I/O also supports LVDS, LVPECL, SSTL18, SSTL2, SSTL3 and PCI signaling levels. The CMOS I/O may also suffice for many low-voltage TTL interfaces depending on specific system requirements.

The cold spare I/O feature allows a part to be powered down (VDDIO/VDD=VSS), have its VDD and VDDIO pins ramped up from VSS, or have its power pins ramped down within a system without loading the active drive on other active parts as long as the I/Os are put in a high-Z state during the power supply transitions. This can enhance overall system lifetime by enabling the replacement of parts that have become defective with redundant cold spare equipped parts. Parts can also be powered down when not needed to minimize the degradation caused by electrical fields and/or to conserve power. This feature is an option for LVCMOS I/O and is present on LVDS inputs.

The tables below summarize the HX5SA I/O options.

HX5SA I/O SUMMARY TABLE

Description	Operating Voltages	Operating Frequency (1)	Features
LVCMOS	1.8V, 2.5V, 3.3V	Up to ~150 MHz	Input, Output, Tri-state, Bi-directional, Pad Pull, Cold Spare, Schmitt, Drive strength, Pad pull
PCI	3.3V	33MHz / 66MHz	Input, Output, Tri-state, Bi-directional, 33MHz, 66MHz
SSTL	1.8V, 2.5V, 3.3V	Up to 250 MHz	Class I & II, Input, Output, Tri-state, Bi-directional, Terminated or Unterminated
LVDS	2.5V, 3.3V	600 Mb/s	Input, Output, Cold Sparing, Terminated or unterminated
LVPECL	3.3V	Up to 1.2GHz (Clock) Up to 1.2Gb/s (Data)	Input, Output, DC Coupled

Notes

(1) System level speeds may be slightly different based on impacts from the transmission line medium.

ASIC METHODOLOGY AND CAD TOOLS

The design flow infrastructure for HX5SA ASICs has been developed by Honeywell and Synopsys. This design environment includes:

- Leading-edge Synopsys EDA tools for designing and verifying complex ASICs
- A flexible set of front-end and back-end design services from design teams expert in the implementation of advanced ASICs and the HX5SA design flow
- Access to intellectual property (IP) cores from Honeywell and Synopsys' DesignWare® IP, to accelerate design time and reduce development costs.

Along with support for traditional and expanded ASIC handoff options, implementation support may include design services available from Honeywell and in a fully collaborative design model.

ASIC Development Flow

The ASIC development flow processes a design from the ASIC specification through tested ASIC delivery. For ASIC designs that push the performance envelope, the flow is configured to support preliminary synthesis and place and route, termed "advanced prove-out", to converge on an optimized design which meets all the performance constraints. The requirements associated with packaging and test are also addressed as part of the ASIC development.

Design For Test (DFT)

Honeywell has integrated Design For Test (DFT) into the HX5SA ASIC Development Flow. It encompasses Memory Built In Self Test (MBIST), Scan/Boundary Scan, ATPG, and Functional test. It is designed to be a complete test process that allows for simulation and hardware test to use the same functional test vectors. The DFT flow is supported by tools from Mentor Graphics, Synopsys and Credence.

TEST CAPABILITIES

Honeywell HX5SA test capabilities include wafer and packaged part level testing. Testing capabilities encompass the complete Class Q and V screening flows. The test platform is based on testers manufactured by Credence among others and includes the EXA3000-800 digital tester.

The EXA3000-800 has a maximum of 1024 digital I/O pins. These consist of 960 channels that are single-ended and have a maximum data rate of 800Mbps. It also has 32 differential channels supporting rates up to 3.2Gbps data rates.

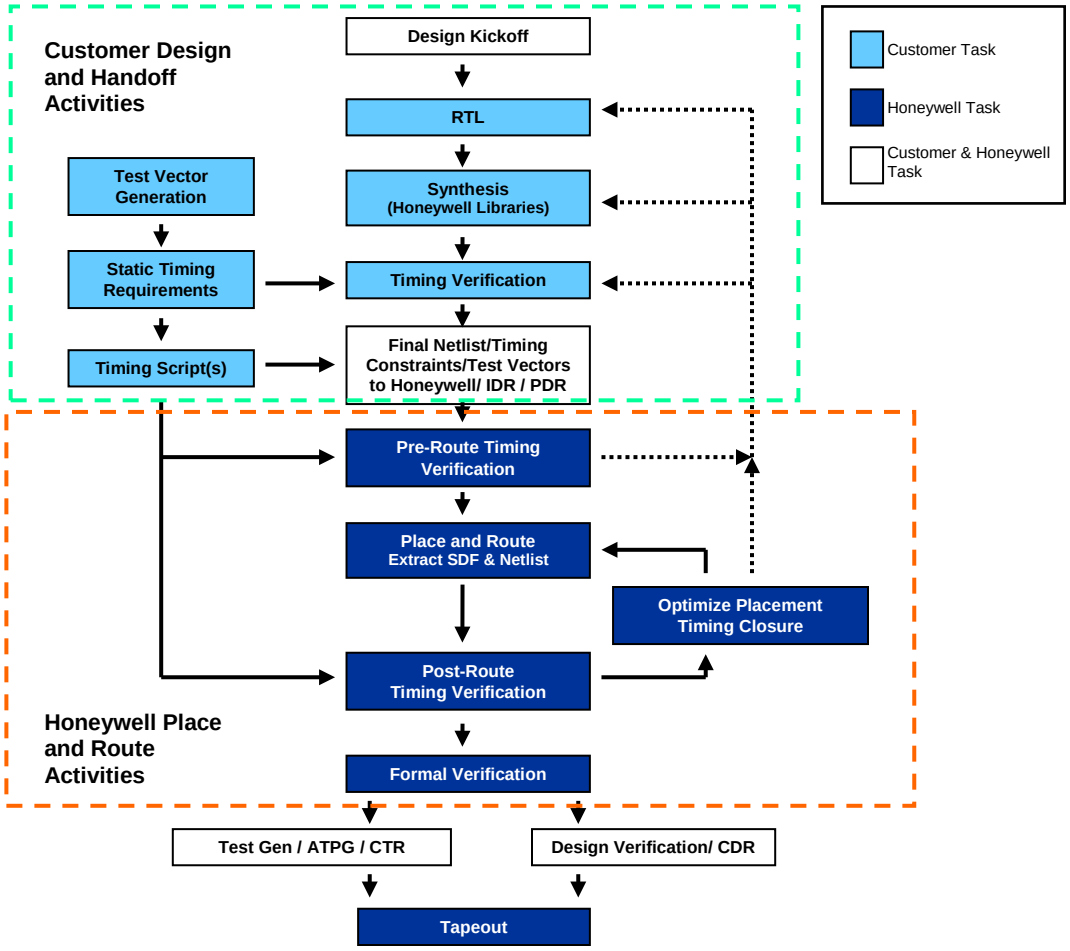
This tester has pin and system level Precision Measurement Units (PMU), timing measurement unit, Sequencer Per Pin (SPP) pattern generator used for digital functional testing, and a 3.2Gbps Wavecrest SIA.

The EXA3000 test system is also designed to support true mixed-signal test techniques using a patented analog channel architecture that is integrated with the digital sub-system. It is equipped with two BroadBand Channel (BBC) instruments and a High Accuracy (HA) instrument.

HX5SA DEVELOPMENT FLOW DIAGRAM

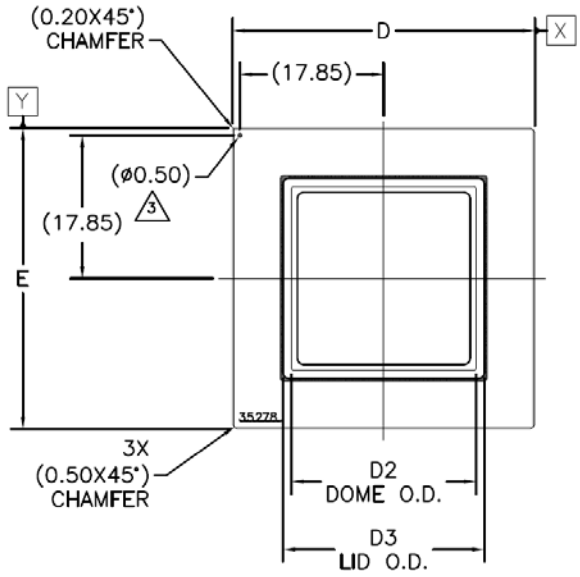
Honeywell uses an industry standard design flow, shown in the figure below. Synthesis libraries are provided for Synopsys Design Compiler. Libraries are provided for Verilog logic simulation. Multiple entry points are available for dividing tasks between Honeywell and the customer, a common one is shown in this figure.

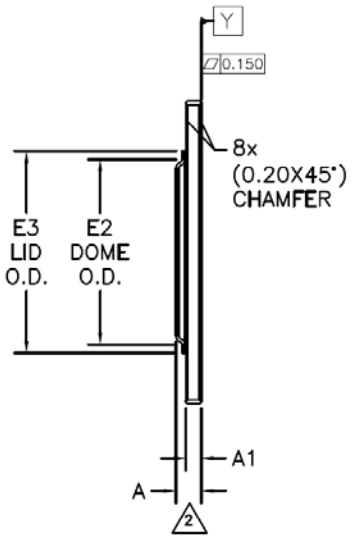
In the flow shown, the designer performs the RTL coding, synthesis, pre/post-route timing and functional verification. Honeywell performs the entire back end layout, timing convergence and test program generation.

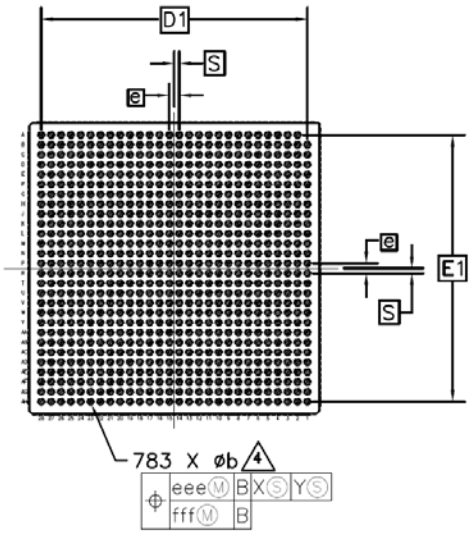


PACKAGING

The HX5SA10 is available in a 783 pin Ceramic Land Grid Array (CLGA).







DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.76	3.07	3.41	.109	.121	.134
A1	1.71	1.90	2.09	.067	.075	.082
b	0.79	0.84	0.89	.031	.033	.035
D/E	37.12	37.50	37.88	1.461	1.476	1.491
D1 E1	34.29			1.350		
D2/E2	22.78	22.92	23.04	.897	.902	.907
D3/E3	24.87	25.00	25.12	.979	.984	.989
e	1.27			0.050		
S	0.635			0.025		
eee	0.30			0.012		
fff	0.15			0.006		

RELIABILITY

For more than 20 years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered thousands of QML parts since first becoming QML qualified in 1990.

Using this proven approach Honeywell will assure the reliability of the S150 products. This approach includes adhering to Honeywell's General Manufacturing Standards for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, negative bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- A statistically controlled wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- The use of characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

QUALIFICATION AND SCREENING

The S150 technology has been qualified by Honeywell after meeting the criteria of the Honeywell General Manufacturing Standards. This approval is the culmination of years of development and requires a considerable amount of testing, documentation, and review. The S150 technology and HX5000 ASIC technology are QML Qualified. This requires additional testing, documentation, and DLA Land and Maritime approval.

The test flow includes screening units with the defined flow (Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups B, C, D, and E). Both the S150 process and individual product are subject to period or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests, respectively.

Periodic qualification and testing at Honeywell and Suppliers address the following requirements.

Group A	General Electrical Tests
Group B	Mechanical - Bond Strength, Solvents, Die Shear
Group C	Life Tests - 1000 hours at 125^{O}C or equivalent
Group D	Package related mechanical tests - Dimensions, Mechanical Shock, Vibration, Acceleration, Seal, Temp Cycle, Thermal Shock, Moisture Resistance, Salt, Lead Integrity, Lead Finish Adhesion, Solderability, Internal Water Vapor, Solder Heat
Group E	Radiation Tests

Honeywell delivers products that are tested to meet your requirements. Products can be screened to several levels including Proof of Design (POD), Engineering Models (EMs), and Flight Units. PODs and EMs are available with limited screening for prototype development and evaluation testing.

For further questions, please call for applications support at 800-323-8295 (USA toll free) or 763-954-2474 or visit our website www.honeywell.com/microelectronics.

Honeywell International Inc.
Aerospace Plymouth
12001 Highway 55
Plymouth, MN 55441
1-800-323-8295
www.honeywell.com/microelectronics

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