

HIGH PERFORMANCE (SOI) GATE ARRAYS

HX3000 FAMILY

FEATURES

- Fabricated on Honeywell's Radiation Hardened 0.28 μm L_{eff} RICMOS™ V SOI Process
- Array Sizes to 1M Usable Gates
- 3.3V or 2.5V Core Operation
- Mixed Voltage I/O Power Supply (2.5V, 3.3V)
- CMOS, PCI, Schmitt Trigger, LVDS, 5V Tol I/O
- Single- or Multi-Port Gate Array SRAM
- Single- or Multi-Port Custom SRAM Drop-In Capability
- Supports Chip Level Power Down for Cold Sparring
- On-Chip Analog Phase Locked Loop (PLL)
- Maximum Clock Rates >250 MHz
- Total Dose Hardness 3x10⁵ rad(SiO₂)
1x10⁶ rad (SiO₂) Option Available
- Soft Error Rate 1x10⁻¹⁰ Errors/Bit/Day
- No Latchup
- Ultra Low Power
0.14 μ W/Gate/MHz (3.3V)
0.08 μ W/Gate/MHz (2.5V)
- Options:
 - Standard Cell ASIC
 - High Density I/O

GENERAL DESCRIPTION

The HX3000 gate array is a performance oriented sea-of-transistor array, fabricated on Honeywell's Silicon-On-Insulator (SOI) RICMOS V process. Very high density is achieved using local interconnect and a 4-layer metal process, providing up to one million usable gates. The high density and performance characteristics of the SOI-V process enable device operation beyond 250 MHz over the full military temperature range, even after exposure to ionizing radiation. Flip-flops have been designed for a Soft Error Rate (SER) of less than 1x10⁻¹⁰ errors/bit/day in the Adams 90% worst case environment.

Each HX3000 design is based on our proven Radiation Insensitive CMOS (RICMOS™) ASIC library of SSI and MSI logic elements, configurable RAM cells, and selectable I/O pads. The gate arrays feature low skew clock distribution. This family is fully compatible with Honeywell's high reliability screening procedures and consistent with QML Class Q and V requirements.

Designers can choose from a wide variety of I/O types. Buffer options include multiple drive strengths, three-state capability, IEEE 1149.1 boundary scan and pull-up/pull-down resistors. PCI compatible buffers are also supported.

The HX3000 product family supports dual voltage I/O. The designer has the flexibility to specify either voltage supply for each I/O site.

Each HX3000 array features an on-chip Phase Locked Loop (PLL) for clock deskewing and frequency multiplication. The PLL requires no external components.

The HX3000 family has a special feature to allow a chip level power down mode, in which the associated buses connected to the chip can remain active. This high impedance off-state buffer feature allows users to power down portions of their system for power savings or for cold sparing.

The HX3000 family provides options for configurable multi-port SRAMs. A variety of SRAM read and write port options are available to serve a wide range of applications. Custom drop-in RAMs can further increase chip density.

ASIC designers need not have prior experience in radiation hardening. Honeywell's VDS™ Design Kit and HX3000 libraries provide the necessary guidance to achieve first pass design success. The VDS Design Kit supports industry standard platforms including those offered by Mentor

HX3000

HX3000 Characteristics (1)	HX303G	HX306G	HX311G	HX314G
Total Core Gate Count (3)	235K	440K	925K	1.2M
Usable Gate Count	210K	380K	790K	1M
Maximum Die I/O*	176	240	320	388
Typical Intrinsic Delay—2 Input NAND	125 ps @ 3.3V; 165 ps @ 2.5V			
Selectable I/O	Driver, Receiver, Bi-Directional, Three-State			
I/O Interface Levels	CMOS, Schmitt Trigger, PCI, LVDS, 5V Tol			
Typical Power Dissipation, W/Gate/MHz (2)	0.14 @ 3.3V; 0.08 @ 2.5V			
Operating Voltage	3.3V 10%; 2.5V 10%			
Operating Temperature	-55 C to 125 C			
Process Technology	RICMOS™ V SOI			
Minimum Geometry	0.28 μm Leff / 0.35 μm Drawn			
Soft Error Rate (SER)	<1E-10 cell upsets/bit-day (Adams 90% W. C. environment, GEO orbit, 25 mil shielding)			
Total Dose Hardness	>300Krad (SiO ₂) (1Mrad Option Available)			

(1) Projected.

(2) Core logic, 20% activity in combinational logic, clocks active.

(3). Future enhancements will increase gate count.

*Contact Honeywell for additional I/O options.

Graphics, Synopsys and Cadence. Design Kit options include VHDL and Verilog.

Honeywell can perform design translations to the HX3000 arrays from other CAD platforms and ASIC vendors. Our synthesis capabilities allow customers to use familiar CAD tools and libraries to map existing designs to Honeywell library components. Floor-planning, timing-driven placement, clock-tree synthesis, and placement-based optimization is also supported for fast design cycles. A variety of

packaging options including QFP, PGA, BGA and Known-Good-Die (KGD) are also available.

The HX3000 family of gate arrays is the right choice for your high reliability space applications demanding high density, high speed and very low power. For higher logic and I/O density with further power optimization, see Honeywell's RICMOS™ V SOI Standard Cell Library data sheet. To learn more about Honeywell's variety of space components, call us at 1-800-323-8295.

To learn more about Honeywell Solid State Electronics Center, visit our web site at <http://www.ssec.honeywell.com>

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