HIGH TEMPERATURE N-CHANNEL POWER FET

FEATURES

- Specified Over -55 to +225°C
- Output Current up to 1 Amp Continuous
- Typical Input Voltage up to 60V
- Silicon-On-Insulator (SOI)
- 4-Pin Power-Tab Package, 8-Pin Ceramic Dip with Integral Heat Sink or Die Dimensions 4.699 x 2.286 mm

APPLICATIONS

- Down-Hole Oil, Gas and Geothermal Well
- Aerospace and Avionics
- Turbine Engine Control
- Industrial Process Control
- Nuclear Reactor
- Electric Power Conversion
- Heavy Duty Internal Combustion Engines

GENERAL DESCRIPTION

The HTNFET is a high reliability N-Channel Power FET designed specifically for extremely wide temperature range applications such as down-hole instrumentation, aerospace, turbine engine and industrial process control. This power FET is fabricated using a Silicon-On-Insulator (SOI) process that dramatically reduces leakage currents at high temperatures.

High DC current capability combined with low Rds-ON make this component suitable both for DC and switching applications. Typically, parts will operate at +300°C up to a year, with derated performance. All parts are burned in to eliminate infant mortality. Additionally, each part is tested over -55 to +225°C to provide guaranteed performance over the entire temperature band.

FUNCTIONAL DIAGRAM

PACKAGE DIAGRAMS

DIE DIAGRAM
## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS (1, 2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameters</th>
<th>Conditions</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(BR)DSS</td>
<td>Drain-source breakdown voltage</td>
<td>VGS = 0, ID = 100 μADC</td>
<td>55</td>
<td>V</td>
</tr>
<tr>
<td>RDS (on)</td>
<td>Static drain-to-source on-state resistance @ Ta=25°C</td>
<td>VGS = +5VDC, ID = 0.1A</td>
<td>0.4</td>
<td>Ω</td>
</tr>
<tr>
<td>VGS (th)</td>
<td>Gate threshold voltage @ Ta=25°C</td>
<td>VGS = VDS, ID = 100 μA</td>
<td>1.6</td>
<td>2.4</td>
</tr>
<tr>
<td>IGSS</td>
<td>Gate-to-source forward leakage</td>
<td>VGS = +5 VDC</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>IGSS</td>
<td>Gate-to-source reverse leakage</td>
<td>VGS = -5 VDC</td>
<td>-100</td>
<td>nA</td>
</tr>
</tbody>
</table>

### Guaranteed by design

- **Qg** Total gate charge (CGS + CGD)
- **td (on)** Turn-on delay time
- **t r** Rise time
- **td (off)** Turn-off delay time
- **t f** Fall time
- **Ciss** Input capacitance
- **Coss** Output capacitance
- **Crss** Reverse transfer capacitance

### IDSS vs TEMPERATURE

![Graph showing IDSS vs Temperature](image)

- **IDSS (A)** vs **Temperature (°C)**
  - **VDS = 90 V**
  - **VDS = 50 V**
  - **VDS = 10 V**

### Notes:

1. Typical operating conditions: VDS = 10 V, TA = 25°C.
2. Worst case operating conditions: VDS = 50 V, TA = -55 to 225°C.

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