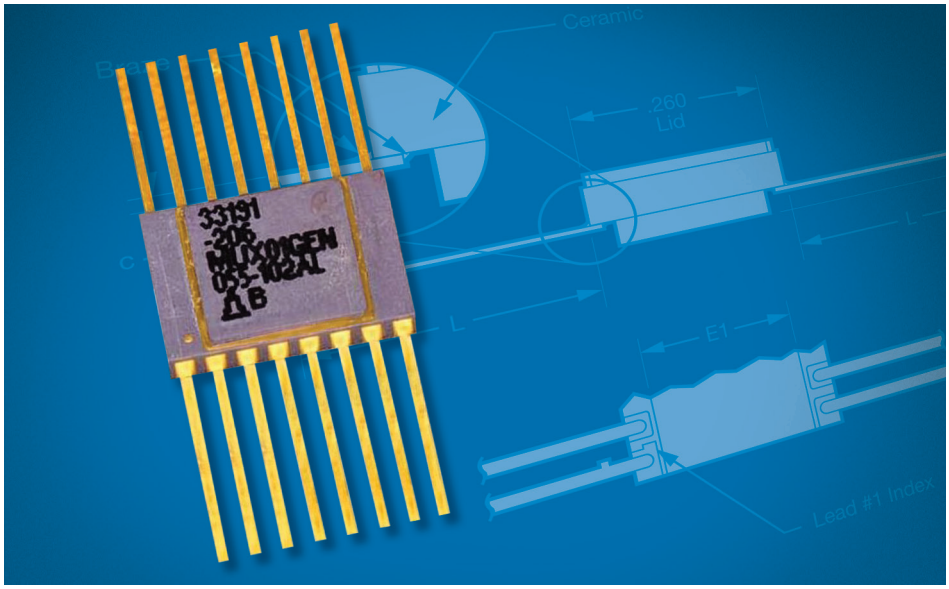
HMXMUX01

Honeywell

8-Channel Analog Multiplexer Radiation Hardened

Features

- Fabricated on Silicon On Insulator (SOI) CMOS Technology
- SOI4 Process (Leff = 0.8 um)
- Total Dose Hardness 300k rad (Si)
- Dose Rate Upset Hardness $1x10^{9}$ rad(Si)/s
- Dose Rate Survivability $1x10^{12}$ rad(Si)/s
- Neutron Hardness $1x10^{14}$ cm^2
- No Latchup
- On Resistance (Ron) Max < 60 Ω
- On Resistance Matching Between Channels (Ron) Max < 20 Ω
- Typical Operating Power ≤ 100 mW
- Guaranteed Break-Before-Make
- Fast Switching
  t_{ON} < 120ns
  t_{OFF} < 120ns
- Operating Range is -55°C to +125°C
- Package: 16 Lead Flat

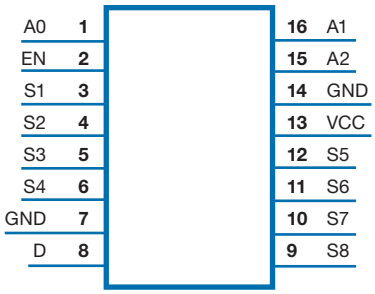


The HMXMUX01 radiation hardened single 8 to 1 multiplexer is a monolithic CMOS analog device designed for high performance and low voltage operation. It is designed to operate from a single +5V supply. It features an inhibit pin to open circuit all signal paths.

All digital inputs have CMOS logic thresholds for simple control with a single +5V supply.

It is fabricated with Honeywell's radiation hardened Silicon On Insulator (SOI) technology, and is designed for use in low-voltage systems operating in radiation environments. The technology enables a low ON Resistance and fast switching times. The 8:1 analog multiplexer operates over the full military temperature range and is operated with 5 ± 0.25V power supply.

Package Pinout



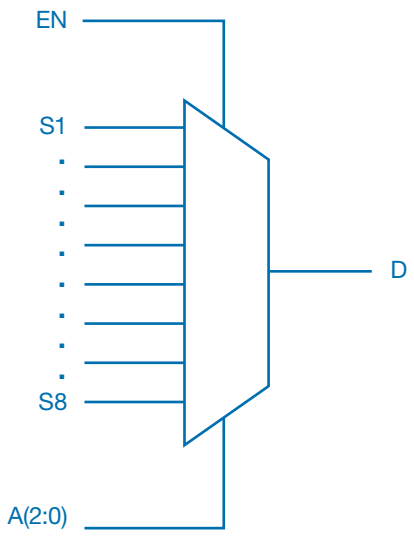
Signal Description

Pin	Signal	Description
1	A0	Digital Input 0
2	EN	Enable
3	S1	Analog Input 1
4	S2	Analog Input 2
5	S3	Analog Input 3
6	S4	Analog Input 4
7	GND	Negative Supply
8	D	Analog Output
9	S8	Analog Input 8
10	S7	Analog Input 7
11	S6	Analog Input 6
12	S5	Analog Input 5
13	VCC	Positive Supply
14	GND	Negative Supply
15	A2	Digital Input 2
16	A1	Digital Input 1

Functional Description

The HMXMUX01 is an 8 input analog multiplexer operating from a 5V supply. The operation is break before make when switching input selection. A single enable pin controls all analog inputs.

Simplified Functional Block Diagram



Truth Table

EN	A2	A1	A0	SWITCH ON
H	L	L	L	S1
H	L	L	H	S2
H	L	H	L	S3
H	L	H	H	S4
H	H	L	L	S5
H	H	L	H	S6
H	H	H	L	S7
H	H	H	H	S8
L	X	X	X	All Off

Radiation Characteristics

Total Ionizing Dose Radiation

The device radiation hardness assurance TID level was qualified by ^{60}Co testing per MIL-STD-883 Method 1019 with the exception of overdose and accelerated anneal. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Transient Dose Rate Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. The device will maintain basic functional operation during exposure to a pulse up to the DRU specification. The device will meet functional, timing and parametric specifications after exposure to a pulse up to the DRS specification.

Neutron Irradiation Damage

SOI CMOS is inherently tolerant to damage from neutron irradiation. The device meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup

The device will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

Radiation Hardness Ratings (1)

Parameter	Symbol	Environment Conditions	Limits	Units
Total Dose (2)	TID		300	krad(Si)
Transient Dose Rate Upset	DRU	Pulse width ≤ 20ns	$1x10^{9}$	rad(Si)/s
Dose Rate Survivability	DRS	Pulse width ≤ 20ns	$1 x10^{12}$	rad(Si)/s
Neutron Fluence		1MeV equivalent energy	$1 x10^{14}$	N/cm^2

(1) Device will not latch up due to any of the specified radiation exposure conditions.
(2) Parts tested to 300K rad without accelerated annealing.

Absolute Maximum Ratings (1)(2)

		Limits		
Parameter	Symbol	Min	Max	Units
Supply Voltage	VCC		6.5	Volt
Analog Input Voltage	V_A	-0.5	VCC+0.5	Volt
Analog Input Current	I_A	-50	50	mA
Digital Input Voltage	V_D	-0.5	VCC+0.5	Volt
Current (any pin)		-50	50	mA
Power Dissipation	P_D		100	mW
Thermal Resistance, Junction to Case (3)	θ_{JC}		16.6	°C /W
Storage Temperature	T_{STORE}	-65	150	°C
Junction Temperature	T_J		175	°C
ESD (Human Body Model)	V_{PROT}		250	V
Lead Temperature (Soldering, 10 seconds)	T_{LMAX}		300	°C

(1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.
(2) GND= 0 volts
(3) By analysis

Recommended Operating Conditions (1)(2)

		Limits		
Parameter	Symbol	Min	Max	Units
Positive Supply Voltage	VCC	4.75	5.25	V
Analog Signal Range	V_A	0	5.25	V
High Level Input Voltage (Digital)	V_{IH}	2.4	VCC	V
Low Level Input Voltage (Digital)	V_{IL}	0	0.8	V
Operating Temperature Steady State	T_C	-55	125	°C

(1) All voltages are with respect to GND = 0.0 volts.
(2) Specifications listed in datasheet apply when used under the Recommended Operating Conditions unless otherwise specified.

DC Electrical Characteristic

VCC = 5.0 V ± 5%, GND = 0.0 V, V_{IH} = 2.4 V, V_{IL} = 0.8 V, T_C = -55 °C to 125 °C (unless otherwise specified)

Parameter	Symbol	Min	Max	Units	Conditions
On-Resistance Drain-Source	R_{ON}		60	Ω	VS = 1V or 3.5V, ID = 5mA, VEN = VIH
RDS Matching Between Channels	ΔR_{DS}		20	Ω	VD = 1V or 3.5V,ID = 5mA, VEN = VIH
On-Resistance Flatness	R_{FLAT}		20	Ω	VD = 1V and 2.25V,IS = 5mA, VEN = VIH
Switch Off Leakage Current	I(off)		15	nA	VS = 1V or 4V, VD = 4V or 1V VEN = VIL
Channel On Leakage Current	I_D(on)		15	nA	VS = 1V or 4V, VD = 4Vor 1V, VEN = VIH Sequence Each Switch On
High Level Input Current	IIH	-10	10	µA	VCC=5.25V; Vin = VIH
Low Level Input Current	IIL	-10	10	µA	VCC=5.25V; Vin = VIL
Power Supply Current	ICC		700	µA	VCC=5.0V, all address inputs=0V

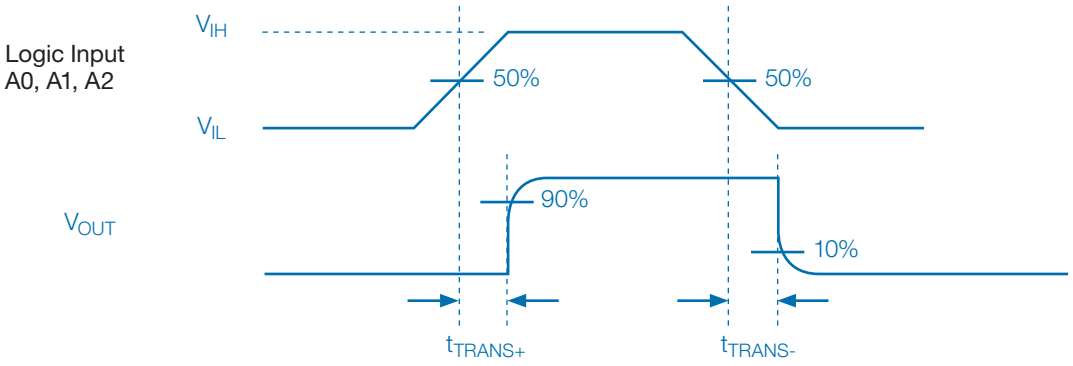
AC Electrical Characteristic (1)

VCC = 5.0 V ± 5%, GND = 0.0 V, V_{IH} = 2.4 V, V_{IL} = 0.8 V, T_C = -55 °C to 125 °C (unless otherwise specified)

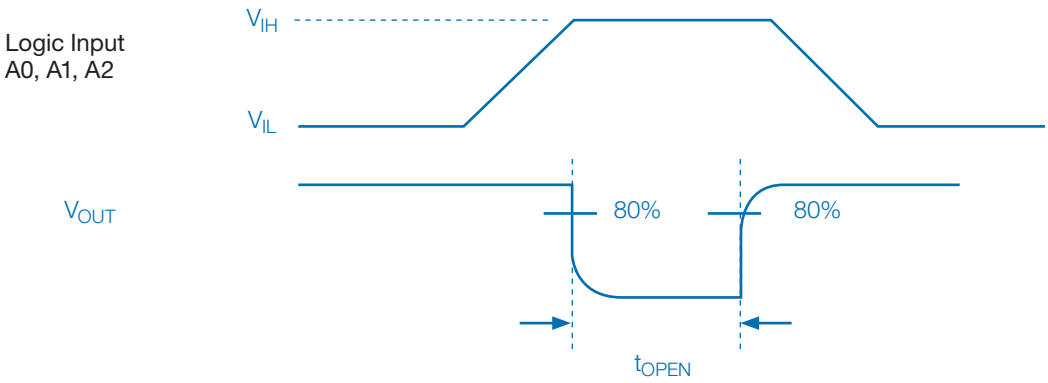
Parameter	Symbol	Min	Max	Units	Conditions
Transition Time	t_{TRANS}		120	nS	V_{S1}, V_{S2}, V_{S3}, V_{S4}, V_{S5}, V_{S6}, V_{S7} = 0 V, V_{S8} = 3.5V, V_{EN} = 3.0 V
Break-Before-Make-Time	t_{OPEN}	10		nS	V_{S1}, V_{S2}, V_{S3}, V_{S4}, V_{S5}, V_{S6}, V_{S7}, V_{S8} = 3.5V V_{EN} = 3.0 V
Enable Turn-On Time	$t_{ON(en)}$		120	nS	V_{S1} = 3.5 V, V_{S2}, V_{S3}, V_{S4}, V_{S5}, V_{S6}, V_{S7}, V_{S8} = 0 V, V_{A0}, V_{A1}, V_{A2} = 0 V
Enable Turn-Off Time	$t_{OFF(en)}$		120	nS	V_{S1} = 3.5 V, V_{S2}, V_{S3}, V_{S4}, V_{S5}, V_{S6}, V_{S7}, V_{S8} = 0 V, V_{A0}, V_{A1}, V_{A2} = 0 V
Charge Injection (2)	Q		20	pC	C_L = 1nF
Off Isolation	OIRR		-65	dB	V_{A0}, V_{A1}, V_{A2}, V_{EN} = 0 V, R_L = 1kΩ
Cross Talk	X_{TALK}		-72	dB	V_{A0}, V_{A1}, V_{A2} = 0 V V_{EN} = 3.0 V, R_L = 1kΩ
Source Off Capacitance (2)	$C_{S(off)}$		10	pF	V_{A0}, V_{A1}, V_{A2}, V_{EN} = 0 V, R_L = 1kΩ
Drain Off Capacitance (2)	$C_{D(off)}$		30	pF	V_{A0}, V_{A1}, V_{A2}, V_{EN} = 0 V, R_L = 1kΩ
Drain On Capacitance (2)	$C_{D(on)}$		30	pF	V_{A0}, V_{A1}, V_{A2} = 0 V V_{EN} = V_{CC}, R_L = 1kΩ

(1) For VCC below 1V, the analog switch impedance is unknown.
(2) These parameters are guaranteed by design. These parameters are not tested by the vendor.

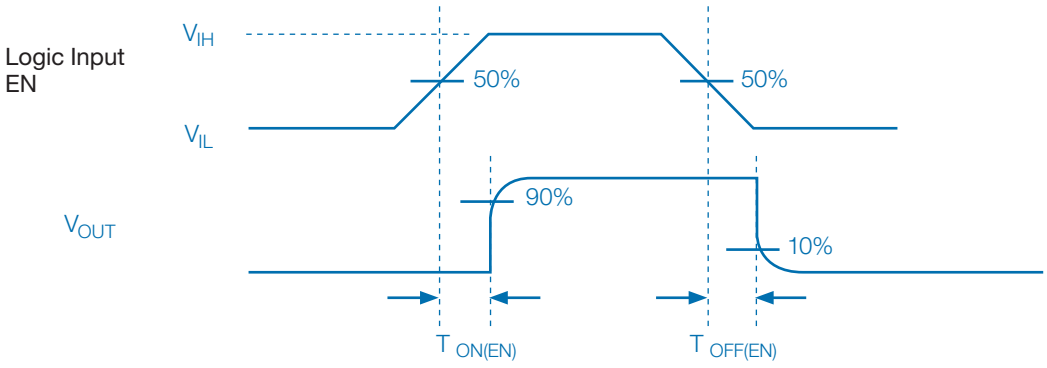
Timing Diagrams



Transition Time



Break Before Make Time (t_{OPEN})



Enable Switching Time

Signal Integrity

As a general design practice, for digital input signals, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns.

Floating inputs for an extended period of time is not recommended.

Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since the early 1990's. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

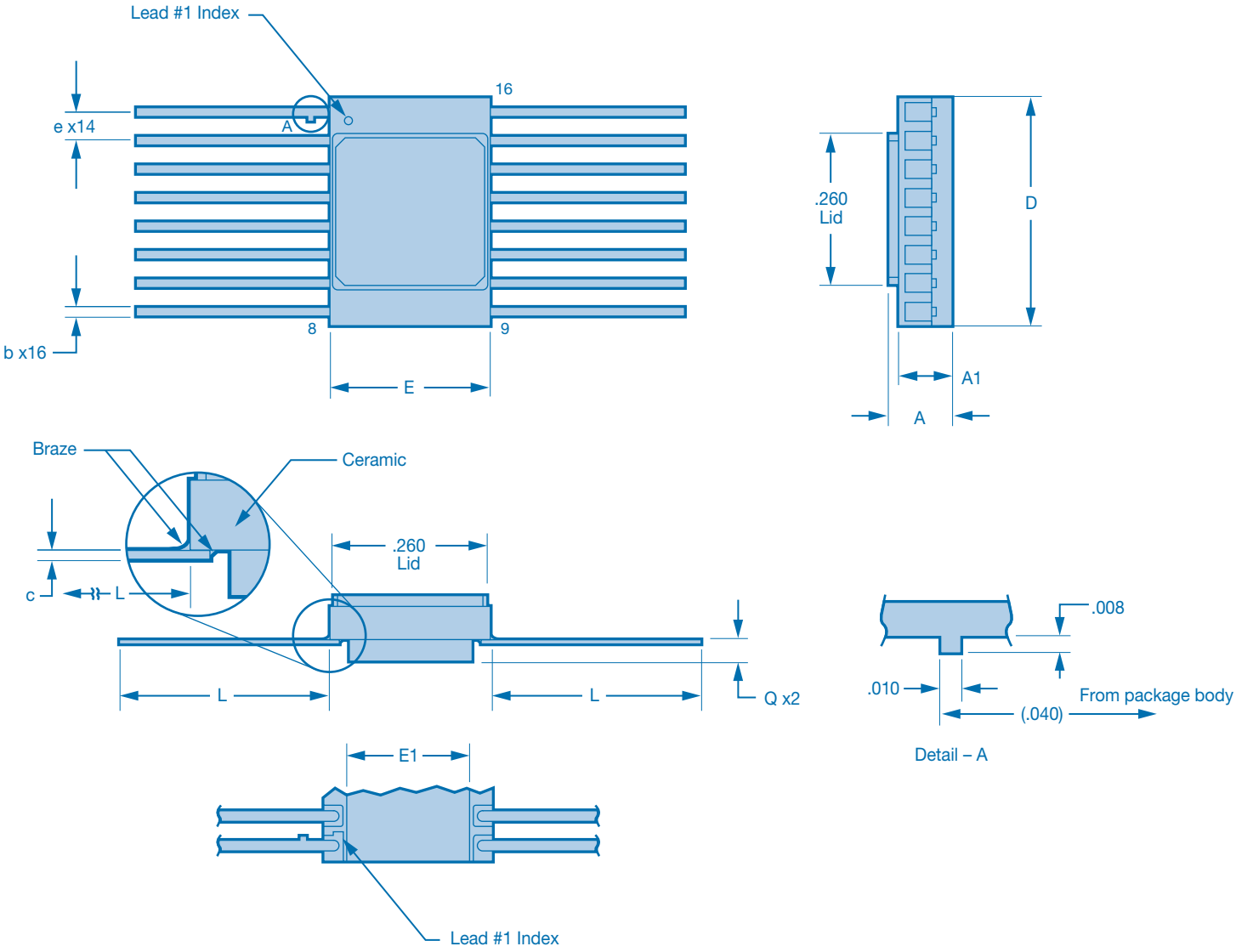
Screening and Conformance Inspection

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Conformance Summary

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

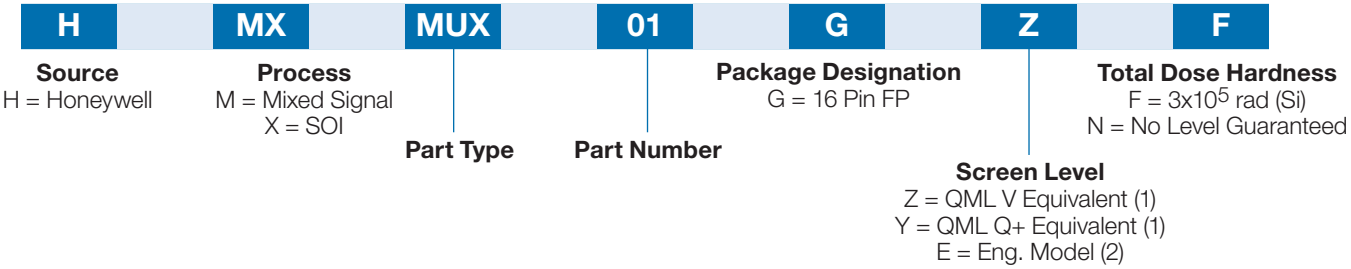
Package Outline Dimensions



1. Controlling dimensions are in inches.

Symbol	Dimensions - Inches			Dimensions - Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	.100	.111	.123	2.54	2.82	3.12
A1	.083	.092	.101	2.11	2.34	2.57
b	.015	.017	.019	0.38	0.43	0.48
c	.004	.005	.007	0.10	0.13	0.18
D	.392	.400	.408	9.96	10.16	10.36
E	.275	.280	.285	6.99	7.11	7.24
e	.047	.050	.053	1.19	1.27	1.35
E1	.199	.205	.211	5.05	5.21	5.36
L	___	.340	___	___	8.64	___
N	___	16	___	___	16	___
Q	.031	.035	.039	0.79	0.89	0.99

Ordering Information (1)



(1) This is an equivelent screening flow but not QML qualified.
(2) Engineering Model Description: Parameters are tested from -55°C to 125°C, 24-hour burn-in, no radiation guarantee.

QCI Testing (1)

Classification	QCI Testing
QML Q+ Equivalent	No lot specific testing performed. (2)
QML V Equivalent	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell Quality Management Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Find out more

To learn more about Honeywell's radiation hardened integrated circuit products and technologies, visit www.honeywellmicroelectronics.com/

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ADS-14199 rev. B
June 2014