Application Note – AN310a
Lead-Free QFN Surface Mount Application
Quad Flat No-Lead Package

UPDATE: August 2011

This application note has been updated to reflect the change to the package. The change included going to a "full-etch" lead type and adding a silver flash plating with the NiPdAu. There is a change in the part number suffix going from –GR (half-etch) to the –FL (full-etch or full-lead).

INTRODUCTION

The most common package for Honeywell's Microwave products is the V-PQFN (Very Thin Plastic Quad Flat No-Lead) which is a small surface mount package with leads on the bottom. For comparison, a V-PQFN package is less than half the size, has half the thermal resistance, has less than half the inductance, and has less capacitance than the corresponding Thin Scale Small Outline Package (TSSOP). Many of Honeywell's new products have RoHS-compliant lead-free finishes. Small packages and lead-free finishes have special soldering concerns that are briefly discussed below.

QFN PACKAGE FEATURES

- Surface mount package
- Small leadless footprint requires less board space
- Lead-free, RoHS-compliant NiPdAu+Au finish
- Very thin <1mm profile aids strict spatial tolerances
- Large center pad for small thermal resistance θ_{ja}
- Low weight for mobile applications
- Very low inductance, resistance and capacitance for high-speed or Microwave applications

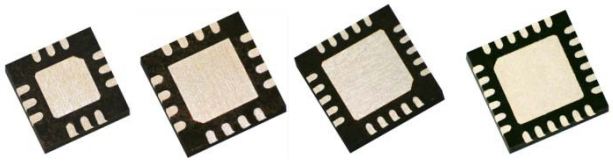

Figure 1
Bottom View of V-PQFN Full-Etch Packages

FULL AND HALF-ETCH PACKAGES

Peripheral leads in half-etch packages are enclosed in mold compound except for the bottom side, are pulled back from the edge of the package and may even be recessed slightly (see Figure 2). The Honeywell –FL QFN packages have full leads - peripheral leads that extend all the way to the package edge on the bottom. The same properly-designed stencil can be used for half-etch and full-lead packages.

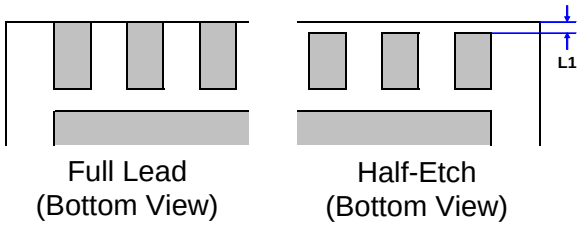

Figure 2
Half-Etch and Full-Lead Bottom View

SURFACE MOUNT RECOMMENDATIONS

The recommended soldering process is to print solder paste on the PCB (Printed Circuit Board) and reflow it after placing components. PCBs should meet the solderability requirements in ANSI/J-STD-003, meet the design requirements in IPC-D-275, and be flat to within 0.1 mm/linear cm. Some of the factors that have a significant effect on mounting QFN packages to the PCB and the quality of the solder joints are:

- Peripheral and center pad stencil design
- Center pad solder paste coverage
- Solder paste and flux type
- Reflow profile, including peak temperature
- Component placement tolerance

LAND PATTERN

The PCB center pad width, D2, should be approximately the same size as the QFN center pad (see Figure 3). The PCB peripheral pad length, Y, should extend beyond the package perimeter of the QFN package lead for fillet formation and to account fabrication and placement tolerances. This length should be approximately 0.15 mm for half-etch parts (-GR) and 0.2 mm to 0.4 mm for full etch parts (-FL). The PCB peripheral pad width, X, should be approximately the same as the QFN package lead and the spacing between PCB peripherals pads should be 0.25 mm minimum to lower the risk of bridging. The minimum required clearance between the PCB center pad outer edge and peripheral pad inner tip to avoid shorts (CPL) is 0.15 mm. The minimum required clearance between PCB center pad row and column to avoid shorts (CLL) is 0.10 mm.

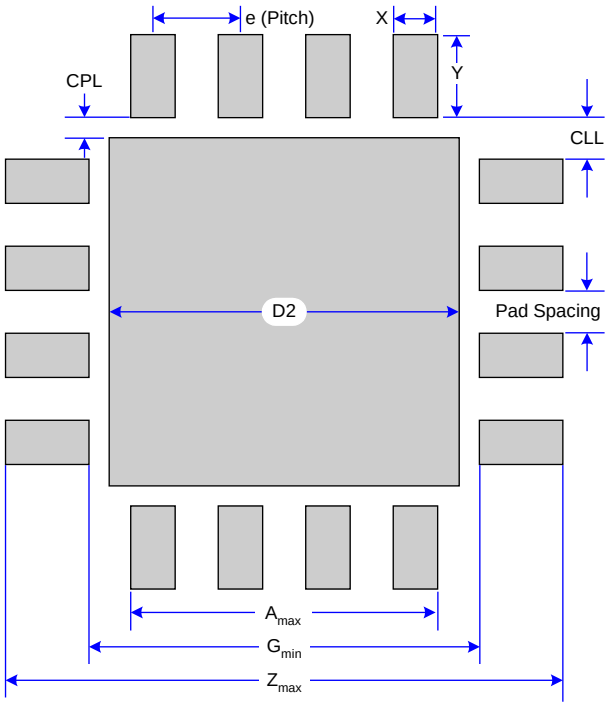

Figure 3
VQFN Land Pattern

STENCIL THICKNESS AND DESIGN

Stencil thickness determines solder paste amount deposited onto the PCB. Too much solder paste will cause solder bridging or excessive standoff. A 0.100 to 0.125 mm (4 to 5 mil) thick stainless steel stencil is recommended for 0.50 mm pitch QFN packages, while a 0.125 to 0.150 mm (5 or 6 mil) thick stencil is allowable for 0.65 mm pitch packages. A step down stencil may be used where the QFN package requires a thinner stencil than other PCB components.

The recommended aperture shape for paste release is trapezoidal. The stencil should be laser cut and electropolished. Smooth stencil surfaces promote better solder paste rolling action and aperture fill. Smooth blades reduce the tendency of solder paste to stick to the surface and build up on the blade holder. Smooth blades also require less pressure to obtain a clean wipe of the stencil resulting in more consistent solder paste volume. Less pressure also reduces the potential for stencil damage thus increasing stencil life.

STENCIL DESIGN FOR PERIPHERAL PADS

The solder and electrical connections to the peripheral pads of the full lead and half-etch packages are designed to be made to the bottom of the QFN packages.

There are two PCB pad designs – Non-Solder Mask Defined (NSMD) and Solder Mask Defined (SMD) pads (see Figure 4). The fine pitch and small outline of the QFN lends itself better to NSMD for peripheral pads as the pad etching process is rather capable and stable allowing smaller pads to be defined accurately. The clearance around the pads and the solder mask should be 0.05 mm minimum and 0.075 mm nominal.

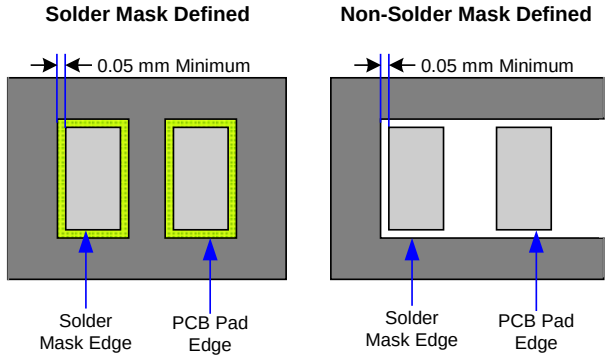

Figure 4
Peripheral Pad Lands and Solder Mask

Aspect and area ratios are key parameters in solder paste printing. The aspect ratio is calculated as the width of the stencil aperture (W) divided by the stencil thickness (T) and should be greater than or equal to 1.5 ($W/T \geq 1.5$). The ratio of the aperture opening area to the aperture wall area should be greater than or equal to 0.6 ($[L*W]/[2*T*[L+W]] \geq 0.66$). Solder mask opening dimensions are recommended to be as tight as possible to ensure that some solder mask remains between the PCB pads.

STENCIL DESIGN FOR CENTER PAD

QFN packages achieve maximum thermal and electrical performance only if the die pad is soldered to the PCB center pad. The PCB center pad should be SMD where the pad area is controlled by the size of the solder mask opening. The solder mask opening for the center pad should be at least 0.065 mm smaller than the PCB center pad on each side.

The solder paste should be printed as an array of multiple small openings at least 0.15 mm apart designed to provide 20 to 50% coverage of the center pad area. This array should ensure good coverage without excessive standoff or bridging to peripheral pads. A high degree of uniformity in solder paste under the center pad will avoid the creation of solder voids that increase the center and electrical resistance.

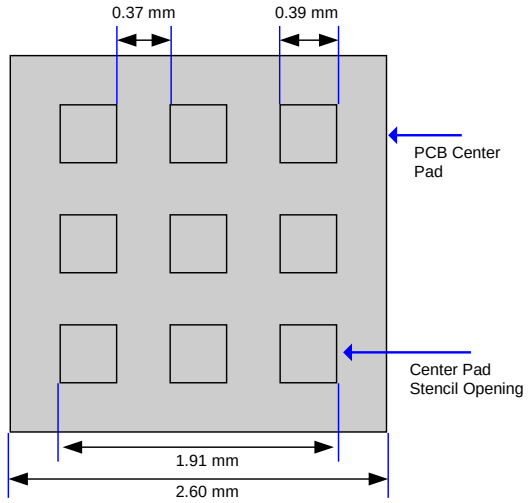

Figure 5a: Example of 20% Stencil Coverage

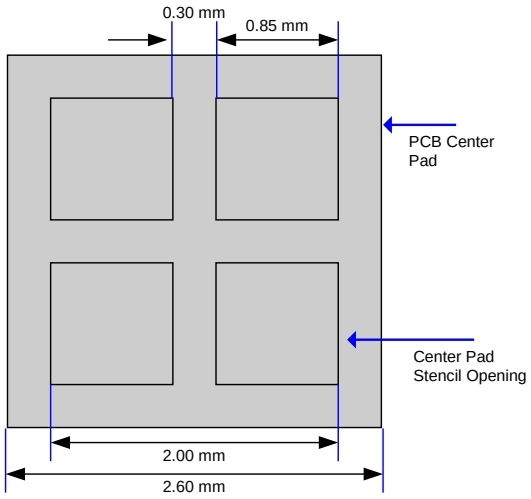

Figure 5b: Example of 43% Stencil Coverage

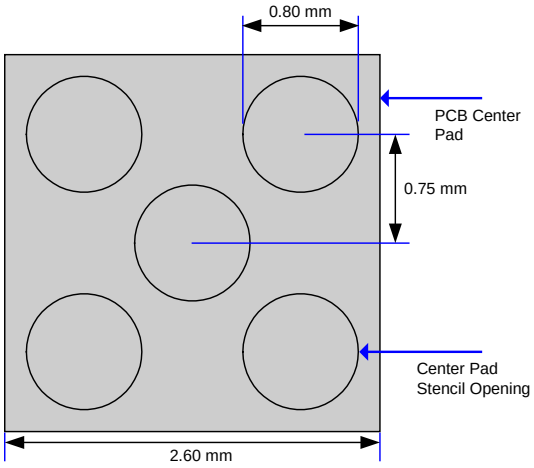

Figure 5c: Example of 37% Stencil Coverage

SOLDER PASTE

Since QFN packages have small peripheral pad openings and minimal standoff height, cleaning after soldering may be difficult. Therefore, no clean Type 3 or similar solder paste may be necessary. A no-clean paste with small particle (powder) sizes works better with fine pitch packages such as the VQFN. Adhesive solder is recommended to aid in restricting part movement during reflow. The JEDEC standard (JESD-B102D) flux for solderability is a standard activated rosin flux (ROL1).

REFLOW PROFILE

The reflow profile should follow the recommendation from the paste supplier. Lead-free solder and NiPdAu finish leads may require a pre-heat between 150 and 200 ºC for 60 to 180 seconds maximum and a peak reflow temperature between 235 and 260 °C with a time above liquidus between 60 to 90 seconds for sufficient flux activation.

Due to the low weight of QFN packages, the airflow may need to be reduced during reflow to prevent parts from shifting or being blown off. The temperature shall be adjusted accordingly to maintain the reflow profile. A nitrogen environment during reflow stops further oxidation but may cause flux bridging between pads.

COMPONENT PLACEMENT

QFN packages are very small, have fine pad pitches, and typically require 0.050 mm package placement tolerance. Using a no-clean flux may necessitate a lower placement pressure to prevent paste smearing or squeezing out of the solder joint. Because of these considerations, high precision component placement machines (ideally with an optical recognition system) are strongly recommended.

TROUBLESHOOTING

QFN PCB SOLDER ISSUE	POTENTIAL RESOLUTION
Excessive standoff leading to lack of peripheral solder connection	Reduce center pad solder paste coverage
	Use a thinner stencil
Some peripheral pads do not sufficiently wet	Use a more active flux
	Increase peak reflow temperature
	Increase pre-heat soak time
	Reflow in a nitrogen environment to limit oxidation
	Adjust reflow temperature for airflow change
QFN package is misaligned after soldering	Reduce package placement tolerance
	Reduce airflow to keep parts from shifting
No side fillet observed (-GR only)	No side fillet is expected as solder connection is only guaranteed to the bottom of the package, not the sides.

For further questions, please call for applications support at 800-323-8295 (USA toll free) or 763-954-2474 or visit our website at www.honeywell.com/microwave.

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