REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct the lead finish designator from “A” to “C” in paragraph 1.2. - CFS	05-03-28	Thomas M. Hess
B	Add case outline Y. - CFS	07-03-05	Thomas M. Hess

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles F. Saffle

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
05-02-18

REVISION LEVEL
B

MICROCIRCUIT, DIGITAL, CMOS, 16-BIT MICROPROCESSOR, MIL-STD-1750 INSTRUCTION SET ARCHITECTURE, MONOLITHIC SILICON

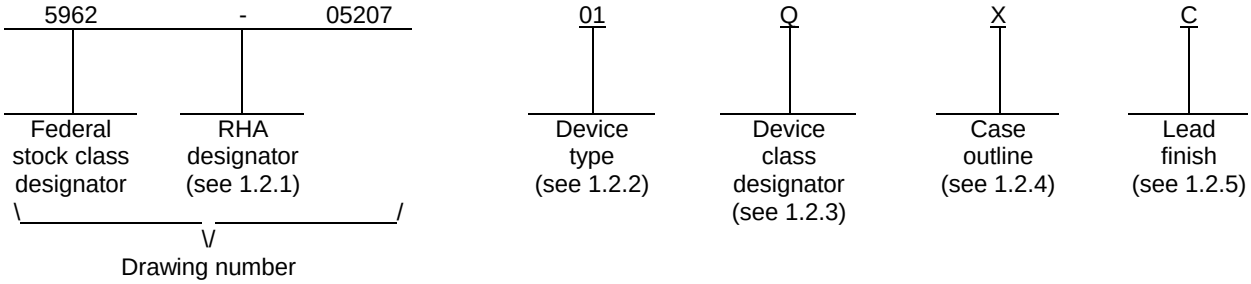
SIZE	CAGE CODE	
A	**67268**	**5962-05207**

SHEET 1 OF 32

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HX1750	16-bit microprocessor with MIL-STD-1750 instruction set architecture, full terminal connection

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA17-P121	121	Pin grid array
Y	See figure 1.	100	Unformed-lead chip carrier
Z	CMGA17-P113	113	Pin grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.5 V dc to +6.5 V dc
Input voltage range (V_{IN})	-0.5 V dc to +6.5 V dc
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+270°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outlines X and Z	See MIL-STD-1835
Case outline Y	2.1°C/W
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D)	1.0 W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Operating frequency (FCLK)	40 MHz
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and as specified on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 4.5 V ≤ V_{DD} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input voltage low 2/	V_{IL}2_50	V_{DD} = 4.5V	1, 2, 3	All		0.8	V
Input voltage high 2/	V_{IH}2_50	V_{DD} = 5.5V			2.0		V
Output voltage low	V_{OL}3_50	V_{DD} = 4.5 V, I_{OL} = 9 mA				0.4	V
Output voltage high	V_{OH}3_50	V_{DD} = 4.5 V, I_{OH} = 9 mA			2.4		V
Input current high, except TSB and D0 - D15	I_{IH}1_50	V_{DD} = 5.5 V, V_{IN} = 5.5 V			-5.0	5.0	µA
Input current high, for TSB and D0 – D15	I_{IH}2_50	V_{DD} = 5.5 V, V_{IN} = 5.5 V			-5.0	5.0	µA
Input current low, except TSB and D0 – D15	I_{IL}1_50	V_{DD} = 5.5 V, V_{IN} = GND			-5.0	5.0	µA
Input current low, for TSB and D0 - D15	I_{IL}2_50	V_{DD} = 5.5 V, V_{IN} = GND			-400	-100	µA
Three-state output current high, except TSB and D0 - D15	I_{OZH}1_50	V_{DD} = 5.5 V, V_{OUT} = 5.5 V			-1.0	1.0	µA
Three-state output current high, for TSB and D0 - D15	I_{OZH}2_50	V_{DD} = 5.5 V, V_{OUT} = 5.5 V			-1.0	1.0	µA
Three-state output current low, except TSB and D0 - D15	I_{OZL}1_50	V_{DD} = 5.5 V, V_{OUT} = 0.0 V			-1.0	1.0	µA
Three-state output current low, for TSB and D0 - D15	I_{OZL}2_50	V_{DD} = 5.5 V, V_{OUT} = 0.0 V			-400	-100	µA
Static V_{DD} supply current	I_{DD}sb_50	V_{DD} = 5.5 V, V_{IN} = 0.0 V or 5.5 V				5	mA
Dynamic V_{DD} supply current	I_{DD}op_50	V_{DD} = 5.5 V, V_{IN} = 0.0 V or 5.5 V Freq = 40 MHz				183	mA
Input capacitance 2/	C_{IN}	See 4.4.1d	4			6	pF
FCLK capacitance 2/	C_{IN}					6	pF
Output capacitance 2/	C_{OUT}					10	pF
STB and SCLK output capacitance 2/	C_{OUT}					17	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{DD} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data Bus input/output capacitance 2/	$C_{I/O}$	See 4.4.1d	4	All		12	pF
Functional tests		See 4.4.1b and 4.4.1c	7, 8				
Hold Tests							
RDY hold from FCLK 3/	t_{HF}(RDY)	See figure 3. 4/ 5/	9, 10, 11	All		2	ns
Data hold from FCLK for a read cycle 3/	t_{HS}(D)R					8	ns
WCODE hold from FCLK 2/ 3/	t_{HS2}(W)S, t_{HS3}(W)S, t_{HF}(W)A					8	ns
CONREQB hold to FCLK 2/ 3/	t_{HLD}(CR)					10	ns
INT0B-INT7B, PWRDNB hold from FCLK 2/ 3/	t_{HS}(INTB)					10	ns
Setup Tests							
RDY setup to FCLK 3/	t_{SUF}(RDY)	See figure 3. 4/ 5/	9, 10, 11	All		3	ns
Data setup to FCLK for a read cycle 3/	t_{SUS}(D)R					0	ns
DMAREQ rise setup to FCLK 3/	t_{RSUS}(DR)					4	ns
DMAREQ fall setup to FCLK 3/	t_{FSUS}(DR)					9	ns
ILLADDB, MPROEB, PEB, PIOXEB setup to FCLK 3/	t_{SUS}(FTB)					18	ns
FTSPARE, BITE setup to FCLK 3/	t_{SUS}(FT)					5	ns
CONREQB setup to FCLK 2/ 3/	t_{SUS}(CR)					20	ns
INT0B-INT7B, PWRDNB setup to FCLK 2/ 3/	t_{SUS}(INTB)					20	ns
WCODE setup to FCLK 2/ 3/	t_{SUS}(W), t_{SUS2}(W)					24	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{DD} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation Delay Tests							
SCLK delay from FCLK 3/	t_{PF}(SCLK)	See figure 3. 4/ 5/	9, 10, 11	All		13	ns
Address delay from FCLK 3/	t_{PS}(AD)					23	ns
ASCSB delay from FCLK 3/	t_{PS}(AS)					22	ns
FLT delay from FCLK 3/	t_{PS}(FLT)					26	ns
Address, ASCSB (no MMU) hold from FCLK 3/ 6/	t_{HS}(A)				5		ns
DI, IOM, DTR, XBO delay from FCLK 3/	t_{PS}(B)					21	ns
DI, IOM, DTR,XBO hold from FCLK 3/ 6/	t_{HS}(B)				5		ns
NOP delay from FCLK 3/	t_{PS}(NOP)					22	ns
STB rise delay from FCLK for a read cycle 3/	t_{RPF}(STB)R					16	ns
DMAK rise delay from FCLK 3/	t_{RPS}(DMAK)					21	ns
SNEW delay from FCLK 3/	t_{PS}(SNEW)					19	ns
Data delay from FCLK for a write cycle 7/	t_{PS}(D)W					48	ns
STB fall delay from FCLK 3/	t_{FPF}(STB)					17	ns
STB rise delay from FCLK for a write cycle 3/ 8/	t_{RPF}(STB)W					13	ns
DMAK fall delay from FCLK 3/	t_{FPF}(DMAK)					19	ns
INTEN, INTKCODE delay from FCLK 3/	t_{PS}(I)					26	ns
DMAEN, INTK, NPU, OD, SUROM, RDOR, RDI, RIC1, RIC2 delay from FCLK 3/	t_{PS}(DIS)					24	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{DD} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation Delay Tests - Continued.							
TRIGOVB delay from FCLK 3/	t_{PS}(TG)	See figure 3. 4/ 5/	9, 10, 11	All		22	ns
Address low Z from FCLK 3/ 9/	t_{LZS}(AD)				7		ns
ASCSB low Z from FCLK 3/ 9/	t_{LZS}(AS)				7		ns
AK low Z from FCLK 3/ 9/	t_{LZS}(AK)				7		ns
Address, AK, ASCSB, DI, IOM, DTR, XBO,valid low Z from TSB 2/ 3/ 9/	t_{LZT}(A,B)				0	75	ns
Data low Z from FCLK for a write cycle 2/ 3/ 9/	t_{LZST}(D)W				0	20	ns
Address, AK, ASCSB, DI, IOM, DTR, XBO valid low Z from DMAK 3/ 9/	t_{LZDM}(A,B)				0	22	ns
Data low Z from TSB 2/ 3/ 9/	t_{LZ}(D)					25	ns
Address high Z from FCLK 3/	t_{HZS}(AD)					20	ns
ASCSB high Z from FCLK 3/	t_{HZS}(AS)					20	ns
AK high Z from FCLK 3/	t_{HZS}(AK)					25	ns
Address, AK, ASCSB, DI, IOM, DTR, XBO valid high Z from DMAK 3/	t_{HZDM}(A,B)					25	ns
Data high Z from FCLK after a write cycle 3/	t_{HZS}(D)W					15	ns
Data hold from STB for a write cycle 3/ 10/	t_H(D)W					10.1	ns
Address, AK, ASCSB, DI, IOM, DTR, XBO valid high Z from TSB 2/ 3/	t_{HZT}(A,B)					75	ns
Data high Z from TSB 2/ 3/	t_{HZ}(D)					25	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{DD} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation Delay Tests - Continued.							
ILLADDB, PEB, MPROEB, PIOXEB, FTSPARE, BITE, INT0B-INT7B pulse width 2/ 3/	t_{PWL}(FI), t_{PWH}(FI)	See figure 3. 4/ 5/	9, 10, 11	All	10		ns
FCLK timing: 3/							ns
Pulse width high	t_{PWH}				10		
Pulse width low	t_{PWL}				10		
Rise and fall time 2/	t_{RF}					5	
Resetb low time 7/ 11/ (f_C = 40MHz)							ns

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ All voltage values are with respect to network ground terminal. Test conditions shall be worst case conditions unless otherwise specified. For AC testing, the device is driven with V_{IL} = 0V and V_{IH} = V_{DD} as specified in table I.

2/ Guaranteed to the limits specified herein if not tested.

3/ f_C = 500 kHz.

4/ Symbol key for AC testing:
- -First letter "t" stands for timing.
- -Second group (subscripted) stands for test type:
  - P = Propagation delay FP = Delay of fall RP = Delay of rise
  - SU = Setup RSU = Setup rise FSU = Setup fall
  - H = Hold
  - PWL = Low pulse width PWH = High pulse width
  - HZ = High impedance delay LZ = Valid low impedance delay
  - RF = Rise and fall time
- -Third group (subscripted) refers to reference signal:
  - F = FCLK
  - ST = The FCLK which causes the transaction of STB
  - S = The FCLK which causes the rise of SCLK
  - S2 = The FCLK following the rise of SCLK
  - S3 = The second FCLK following the rise of SCLK
  - T = TSB
  - SS = SCLK
  - DM = The FCLK which causes the transition of DMAK
- -Letters in parentheses refer to signal tested.
- -Symbols related to read cycles end in "R" whereas the ones related to write cycles end in "W".
- -Symbols related to synchronous cycles end in "S", the ones related to asynchronous cycles end in "A".

5/ Output delay maximum numbers are given for 85 pF load.

6/ These output hold times are tested to assure they are greater than the data input hold times t_{HS}(D)R.

7/ Tested go/no go.

8/ Refers to the FCLK fall, prior to the FCLK rise, which generates the rise of SCLK.

9/ Low Z parameters are measured at V_{DD}/2.

10/ t_H(D)W = ½ period of FCLK or t_{PWL}(FI). t_H(D)W is calculated as the difference between the delay from FCLK falling to data going into three-state and FCLK falling to STB rising.

11/ Minimum RESETB low time is four periods of FCLK.

Case Y

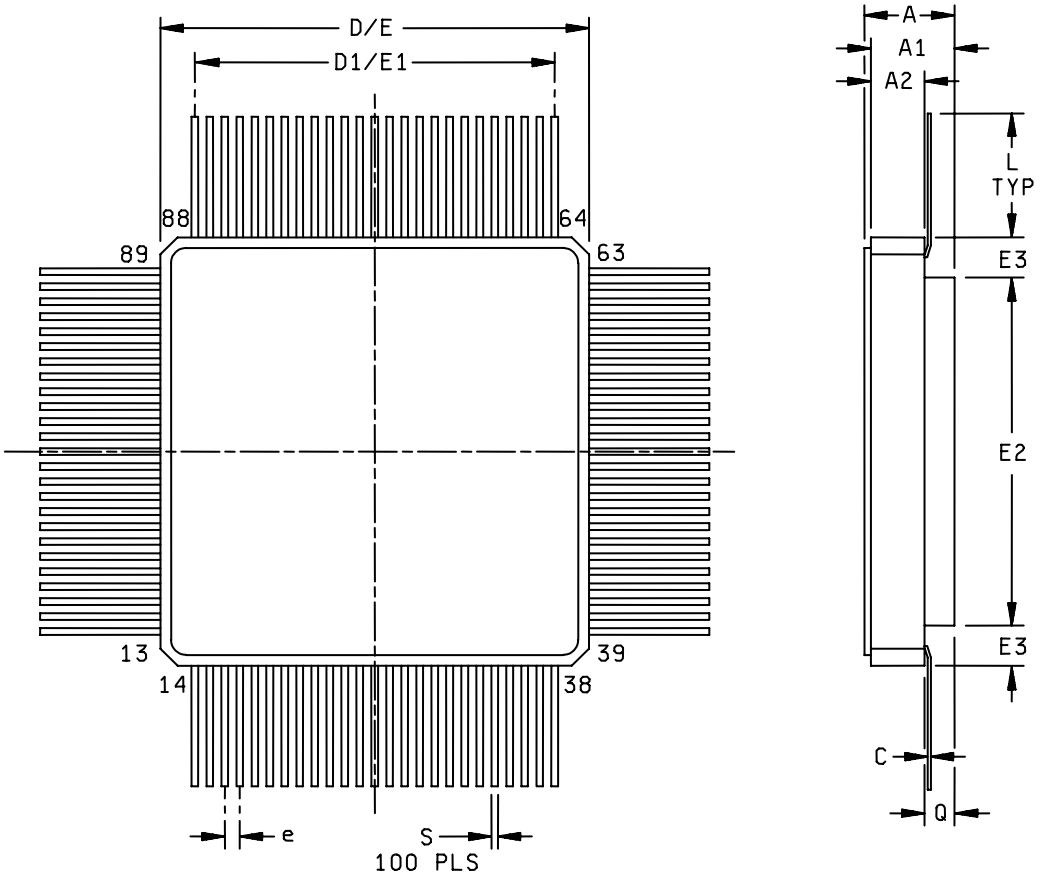


FIGURE 1. Case outlines.

Case Y

Case outline:		Y		
Device type:		01		
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.17		.164
A1	.310	.376	.122	.148
A2	2.16 BSC		.085 BSC	
C	0.10	0.15	.004	.006
D/E	17.45 NOM		.687 NOM	
D1/E1	15.24 NOM		.600 NOM	
E2	14.28	14.58	.562	.574
E3	1.53 NOM		.060 NOM	
e	0.64 NOM		.025 NOM	
L	5.08 NOM		.200 NOM	
Q	1.02 NOM		.040 NOM	
S	0.635 NOM		.025 NOM	

NOTES:
1. All dimensions are in millimeters (inches shown for general reference).
2. Lead finishes are in accordance with MIL-PRF-38535.

FIGURE 1. Case outlines - Continued.

Device type:	01				
Case outlines:	X and Z	Y			
Terminal Mnemonic	Terminal Pin	Terminal Pin	Terminal Name	Terminal Type	Terminal Buffer Description
V_{SS1}	L6	47	Ground 1	GND	
V_{SS2}	C12	88	Ground 2	GND	
V_{DD1}	B2	14	Power 1	VDD	
V_{DD2}	M12	64	Power 2	VDD	
A0	A6	4	Address 0	OZ	No Resistor, 9mA
A1	A7	3	Address 1	OZ	No Resistor, 9mA
A2	C7	2	Address 2	OZ	No Resistor, 9mA
A3	B7	1	Address 3	OZ	No Resistor, 9mA
A4	A8	100	Address 4	OZ	No Resistor, 9mA
A5	B8	99	Address 5	OZ	No Resistor, 9mA
A6	A9	98	Address 6	OZ	No Resistor, 9mA
A7	B9	97	Address 7	OZ	No Resistor, 9mA
A8	A10	96	Address 8	OZ	No Resistor, 9mA
A9	C9	95	Address 9	OZ	No Resistor, 9mA
A10	B10	94	Address 10	OZ	No Resistor, 9mA
A11	A11	93	Address 11	OZ	No Resistor, 9mA
A12	B11	92	Address 12	OZ	No Resistor, 9mA
A13	C10	91	Address 13	OZ	No Resistor, 9mA
A14	A12	90	Address 14	OZ	No Resistor, 9mA
A15	B12	89	Address 15	OZ	No Resistor, 9mA
D0	L10	63	Data 0	B	Pullup, 9mA
D1	N12	62	Data 1	B	Pullup, 9mA
D2	N11	61	Data 2	B	Pullup, 9mA
D3	M10	60	Data 3	B	Pullup, 9mA
D4	L9	59	Data 4	B	Pullup, 9mA
D5	N10	58	Data 5	B	Pullup, 9mA
D6	M9	57	Data 6	B	Pullup, 9mA
D7	N9	56	Data 7	B	Pullup, 9mA
D8	L8	55	Data 8	B	Pullup, 9mA
D9	M8	54	Data 9	B	Pullup, 9mA
D10	N8	53	Data 10	B	Pullup, 9mA
D11	N7	52	Data 11	B	Pullup, 9mA
D12	L7	51	Data 12	B	Pullup, 9mA
D13	M7	50	Data 13	B	Pullup, 9mA
D14	N6	49	Data 14	B	Pullup, 9mA
D15	M6	48	Data 15	B	Pullup, 9mA
ASCSB0	A1	13	Address state 0	OZ	No Resistor, 9mA
ASCSB1	B3	12	Address state 1	OZ	No Resistor, 9mA
ASCSB2	C4	11	Address state 2	OZ	No Resistor, 9mA
ASCSB3	A2	10	Address state 3	OZ	No Resistor, 9mA
AK0	A3	9	Access key 0	OZ	No Resistor, 9mA
AK1	B4	8	Access key 1	OZ	No Resistor, 9mA
AK2	C5	7	Access key 2	OZ	No Resistor, 9mA
AK3	A4	6	Access key 3	OZ	No Resistor, 9mA
DTR	H2	30	Data Tx/Rx	OZ	No Resistor, 9mA
STB	B6	5	Strobe	OZ	No Resistor, 9mA
IOM	H1	29	I/O memory	OZ	No Resistor, 9mA
DI	G1	28	Data/instruction	OZ	No Resistor, 9mA
XBO	G3	27	Extended bus operation	OZ	No Resistor, 9mA

FIGURE 2. Terminal connections.

Device type:	01				
Case outlines:	X and Z	Y			
Terminal Mnemonic	Terminal Pin	Terminal Pin	Terminal Name	Terminal Type	Terminal Buffer Description
TSB	E13	80	Three-state control	I	CMOS, Pullup
DMAREQ	M13	65	DMA request	I	CMOS, No Resistor
DMAEN	D1	21	DMA enable	O	No Resistor, 9mA
DMAK	E3	20	DMA acknowledge	I	CMOS, No Resistor
WCODE0	K11	66	Wait code bit 0	I	CMOS, No Resistor
WCODE1	L12	67	Wait code bit 1	I	CMOS, No Resistor
WCODE2	L13	68	Wait code bit 2	I	CMOS, No Resistor
WCODE3	K12	69	Wait code bit 3	I	CMOS, No Resistor
WCODE4	J11	70	Wait code bit 4	I	CMOS, No Resistor
RDY	D2	19	Bus ready	I	CMOS, No Resistor
INTEN	G12 1/	74	Interrupts enabled	O	No Resistor, 9mA
INTK	D13	82	Interrupt acknowledge	O	No Resistor, 9mA
INTKCODE0	F12 1/	78	Interrupt acknowledge code 0	O	No Resistor, 9mA
INTKCODE1	F13 1/	77	Interrupt acknowledge code 1	O	No Resistor, 9mA
INTKCODE2	G13 1/	76	Interrupt acknowledge code 2	O	No Resistor, 9mA
INTKCODE3	G11 1/	75	Interrupt acknowledge code 3	O	No Resistor, 9mA
INT0B	L1	36	Interrupt 0 (1750 level 2 interrupt)	I	CMOS, No Resistor
INT1B	K2	35	Interrupt 1 (1750 level 8 interrupt)	I	CMOS, No Resistor
INT2B	J3	34	Interrupt 2 (1750 level 10 interrupt)	I	CMOS, No Resistor
INT3B	K1	33	Interrupt 3 (1750 level 11 interrupt)	I	CMOS, No Resistor
INT4B	J2	32	Interrupt 4 (1750 level 12 interrupt)	I	CMOS, No Resistor
INT5B	H3	31	Interrupt 5 (1750 level 13 interrupt)	I	CMOS, No Resistor
INT6B	F1	26	Interrupt 6 (1750 level 14 interrupt)	I	CMOS, No Resistor
INT7B	F2	25	Interrupt 7 (1750 level 15 interrupt)	I	CMOS, No Resistor

FIGURE 2. Terminal connections - Continued.

Device type:	01				
Case outlines:	X and Z	Y			
Terminal Mnemonic	Terminal Pin	Terminal Pin	Terminal Name	Terminal Type	Terminal Buffer Description
PWRDNB	M1	37	Power down (1750 level 0 interrupt)	I	CMOS, No Resistor
FTSPARE	K3	38	Spare fault (FT7)	I	CMOS, No Resistor
PIOXEB	L4	43	PIO transmission error fault (FT6)	I	CMOS, No Resistor
PEB	N2	42	Memory, PIO, DMA, parity error (FT2, FT3, FT4)	I	CMOS, No Resistor
BITE	L3	40	Built-in test error fault (FT13)	I	CMOS, No Resistor
MPROEB	M2	41	Memory protect error fault (FT10, FT1)	I	CMOS, No Resistor
ILLADDB	L2	39	Illegal address fault (FT5, FT8)	I	CMOS, No Resistor
FLT	E2	22	"OR" of fault register (FT5, FT8)	O	No Resistor, 9mA
CONREQB	M5	46	Console request	I	CMOS, No Resistor
RESETB	B1	15	System reset	I	CMOS, No Resistor
SNEW	N4	45	Start new instruction	O	No Resistor, 9mA
SCANEN	E12	81	Scan enable	I	CMOS, No Resistor
SCLK	C1	18	Scan clock	O	No Resistor, 9mA
FCLK	C2	17	Fast clock	I	CMOS, No Resistor
SCALE	K13	71	Clock scale	I	CMOS, No Resistor
TCLK	F3	24	Timer clock	I	CMOS, No Resistor
TGOCLK	D3	16	Trigger GO clock	I	CMOS, No Resistor
RDI	D11	87	Discrete input	O	No Resistor, 9mA
OD	B13	86	Discrete output	O	No Resistor, 9mA
RDOR	C13	85	Read discrete output register	O	No Resistor, 9mA
RIC1	H13 1/	73	Read IOIC interrupt code 1	O	No Resistor, 9mA
RIC2	H12 1/	72	Read IOIC interrupt code 2	O	No Resistor, 9mA
SUROM	D12 1/	84	Start-up ROM enabled	O	No Resistor, 9mA
NPU	E11	83	Normal power up	O	No Resistor, 9mA
TRIGOVB	E1	23	Trigger GO overflow	O	No Resistor, 9mA
DEFCON	L5	44	Default configuration indicator	I	CMOS, No Resistor
NOP	F11 1/	79	Non bus cycle	O	No Resistor, 9mA

1/ Not available in case outline Z.

FIGURE 2. Terminal connections - Continued.

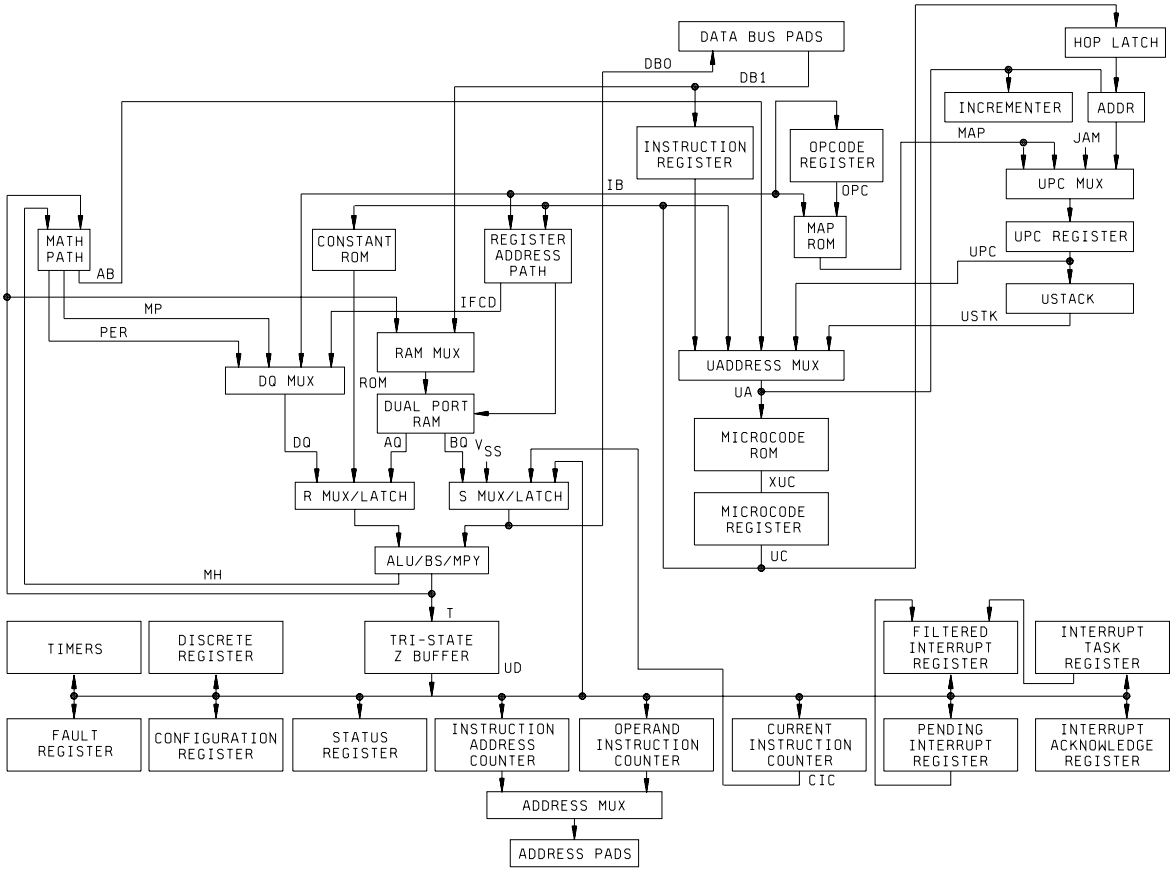


FIGURE 3. Functional block diagram.

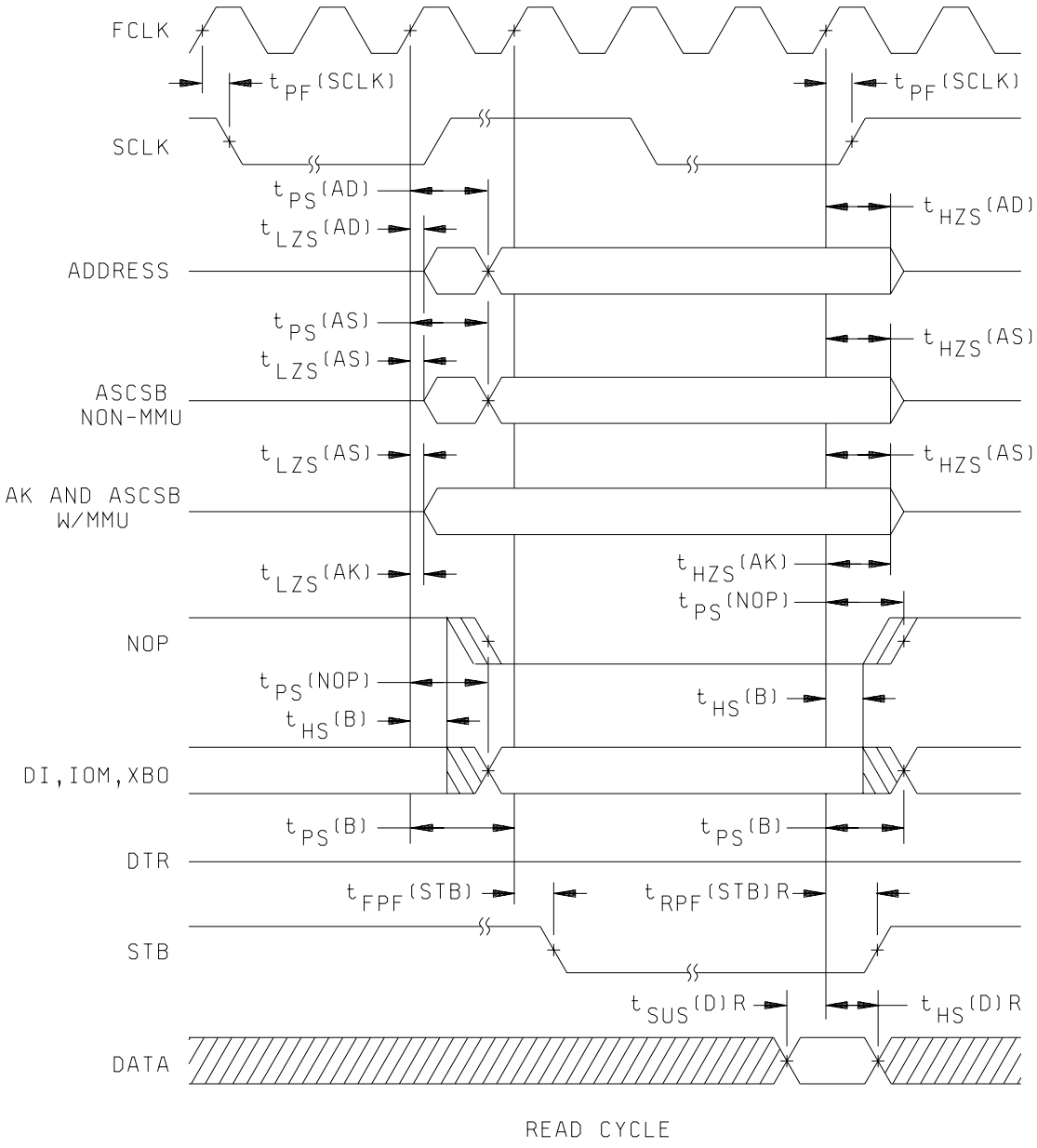


FIGURE 4. Timing waveforms.

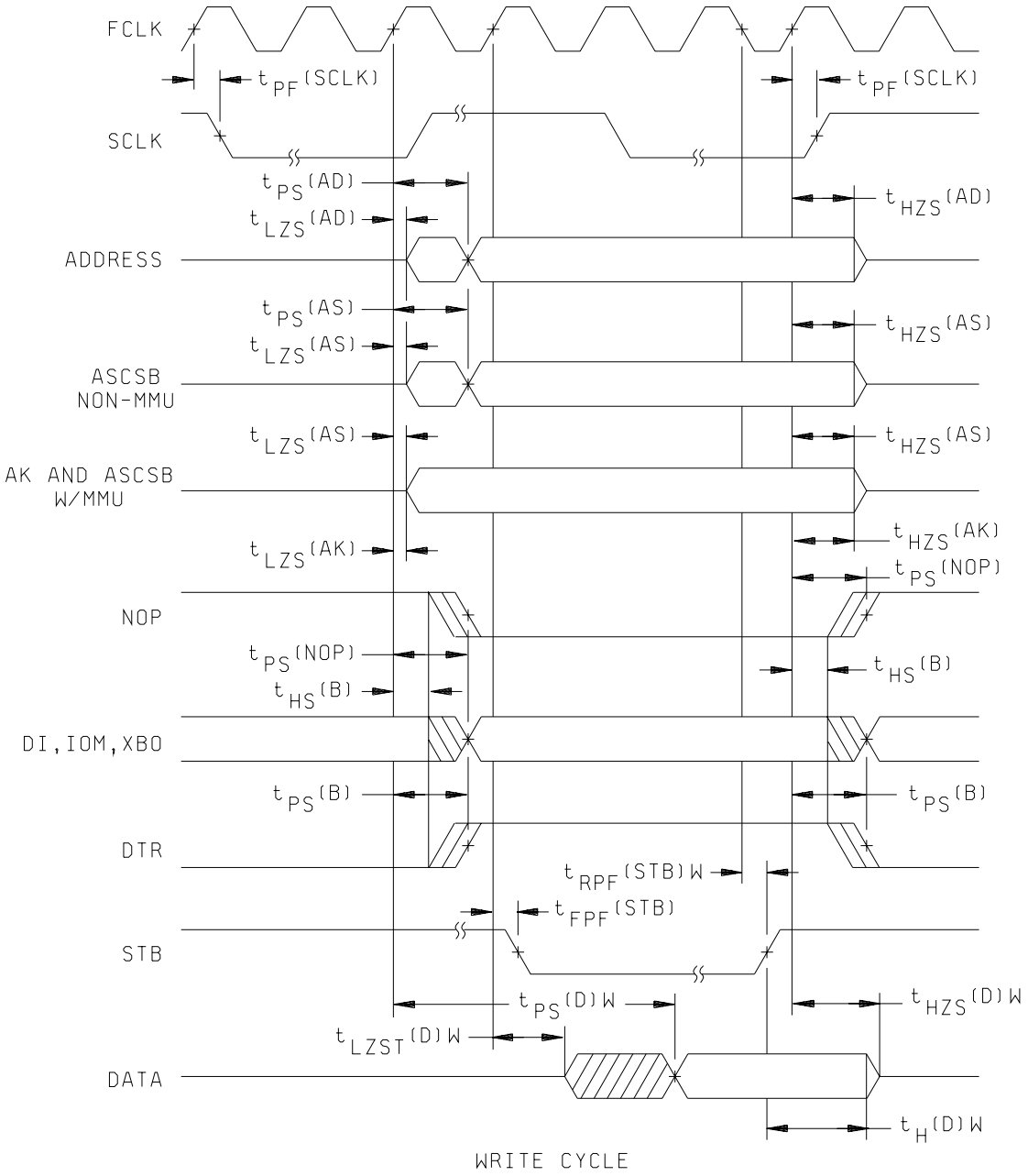


FIGURE 4. Timing waveforms - Continued.

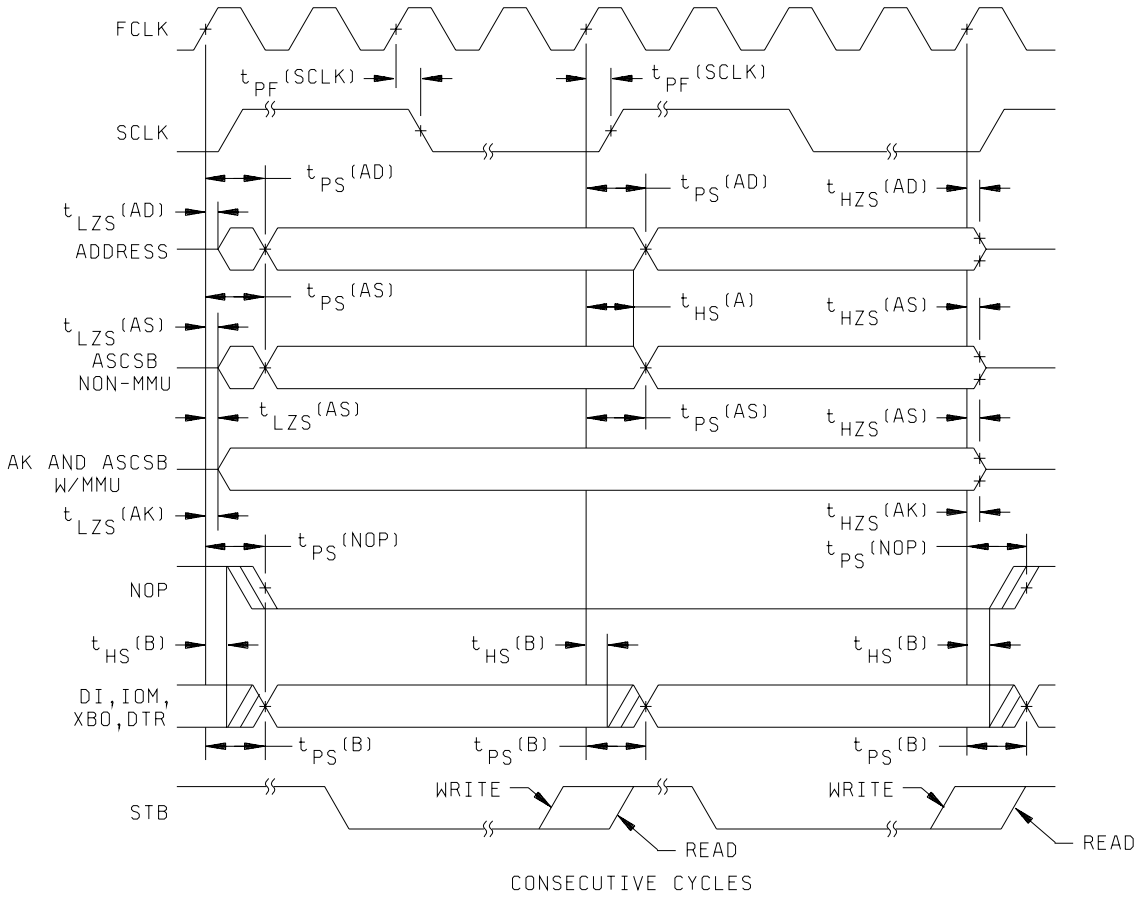
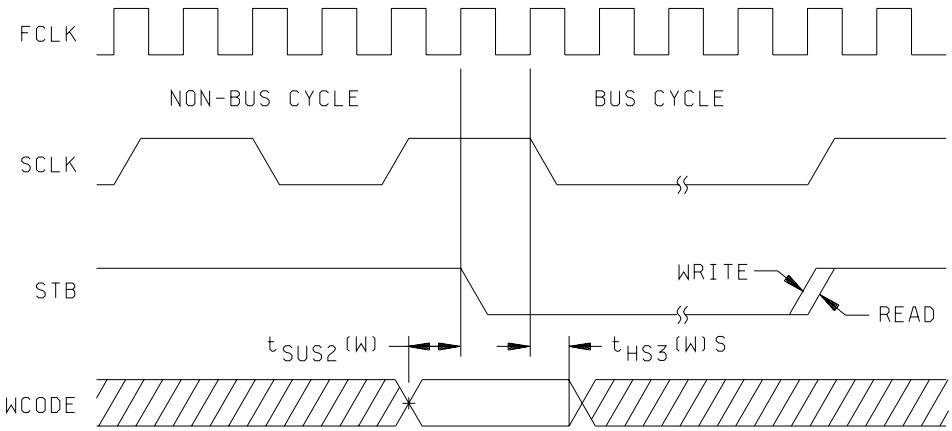
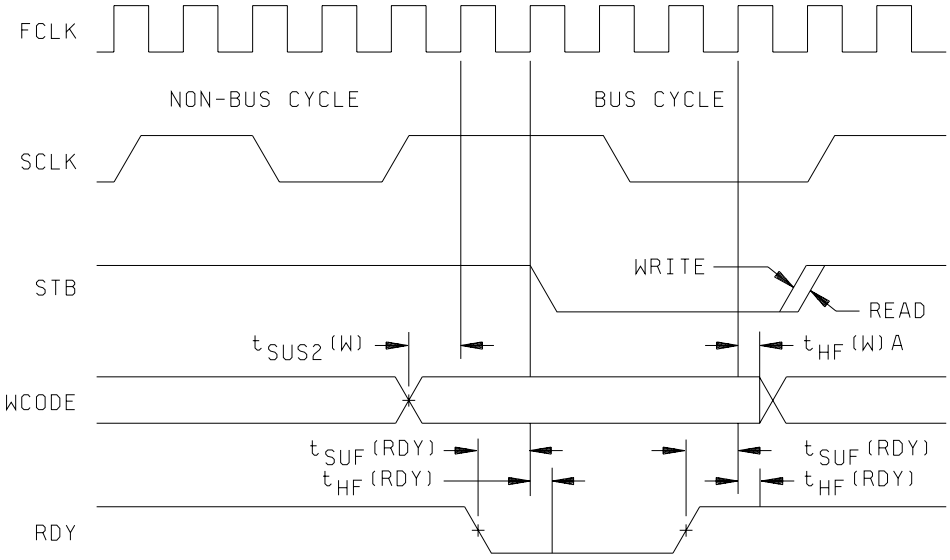


FIGURE 4. Timing waveforms - Continued.

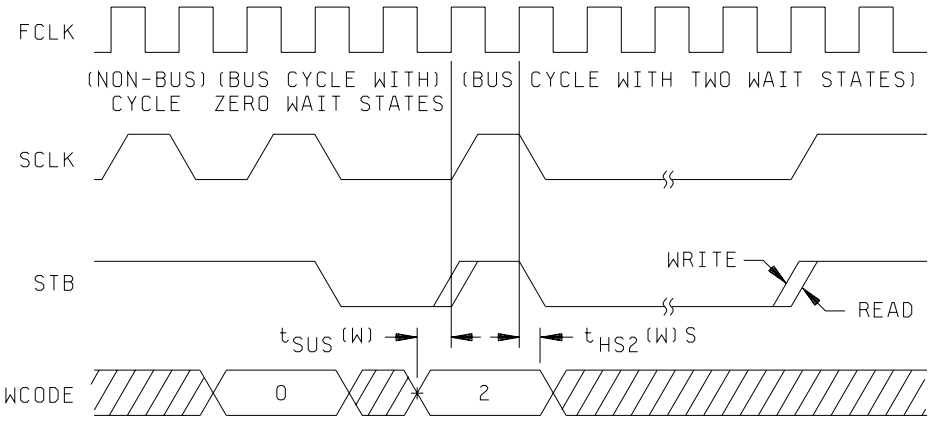


CYCLE CONTROL-SCALE 0-EXAMPLE SHOWS TWO WAIT STATES ADDED SYNCHRONOUSLY

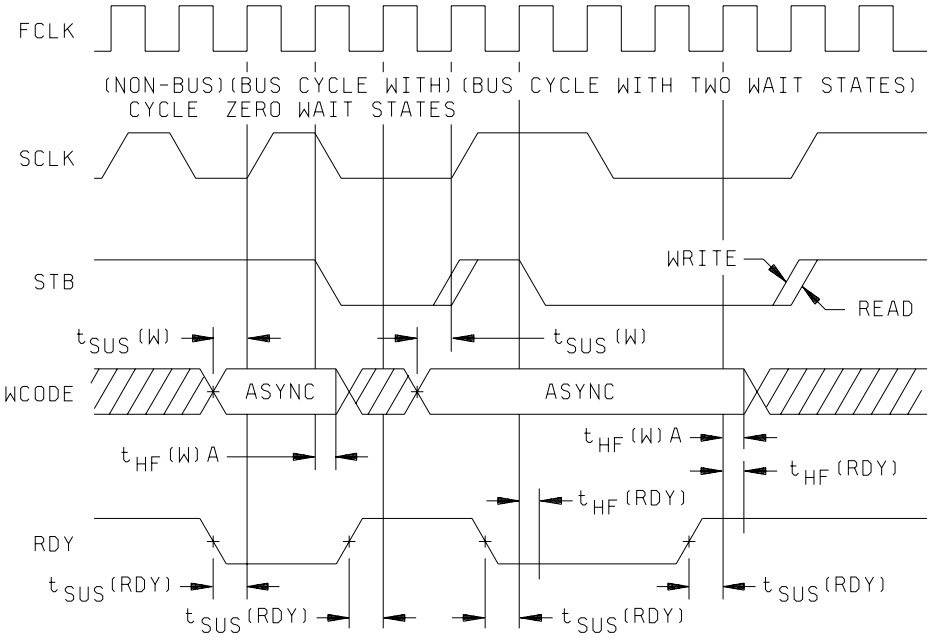


CYCLE CONTROL-SCALE 0- EXAMPLE SHOWS ONE WAIT STATE ADDED TO SCLK HIGH AND ONE WAIT STATE ADDED TO SCLK LOW ASYNCHRONOUSLY

FIGURE 4. Timing waveforms - Continued.



CYCLE CONTROL-SCALE 1-EXAMPLE SHOWS A ZERO WAIT STATE CYCLE FOLLOWED BY ONE WITH TWO WAIT STATE ADDED SYNCHRONOUSLY



CYCLE CONTROL-SCALE 1-EXAMPLE SHOWS A ZERO WAIT STATE CYCLE FOLLOWED BY ONE WITH ONE WAIT STATE ADDED TO SCLK HIGH AND ONE WAIT STATE ADDED TO SCLK LOW ASYNCHRONOUSLY

FIGURE 4. Timing waveforms - Continued.

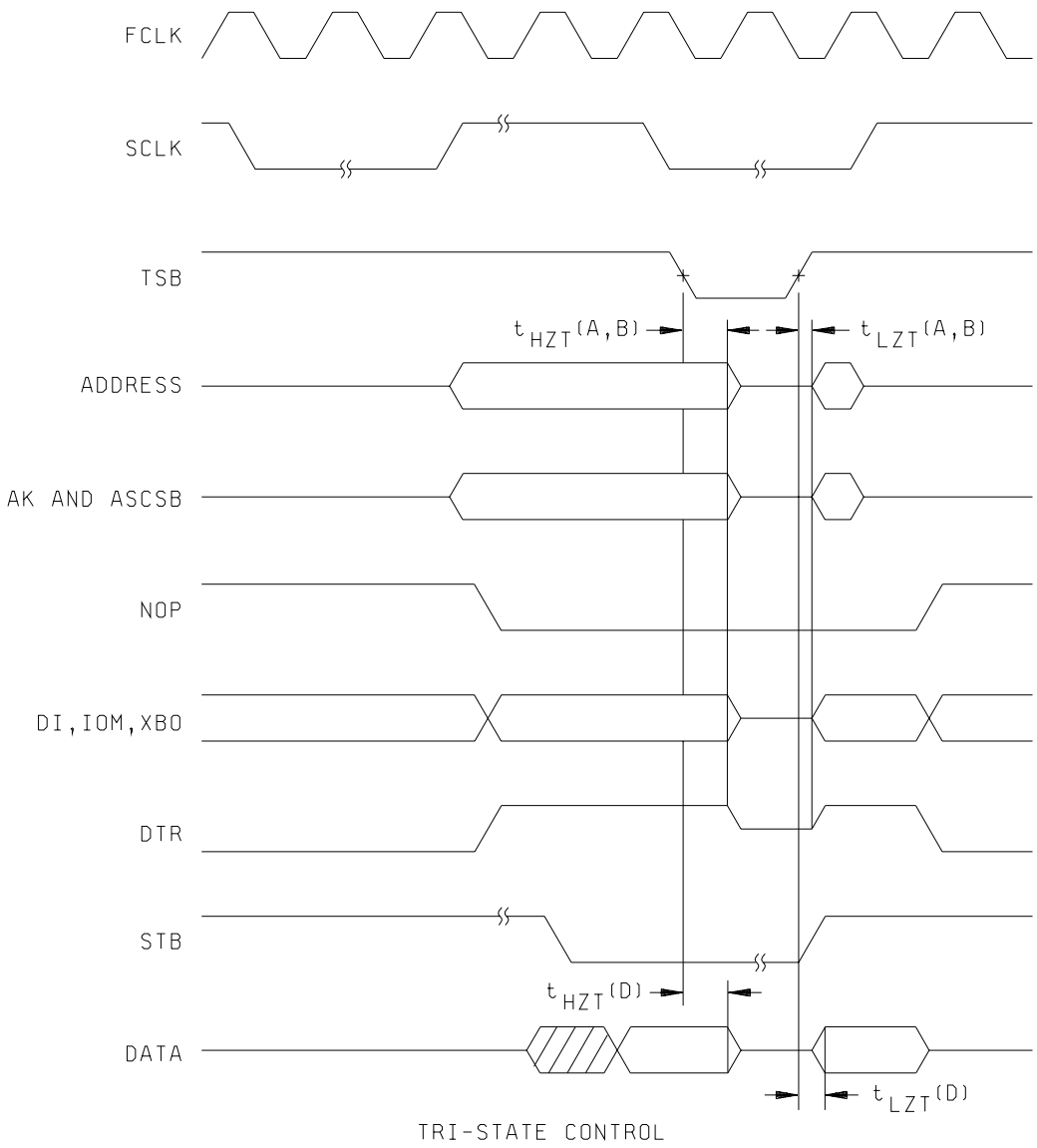


FIGURE 4. Timing waveforms - Continued.

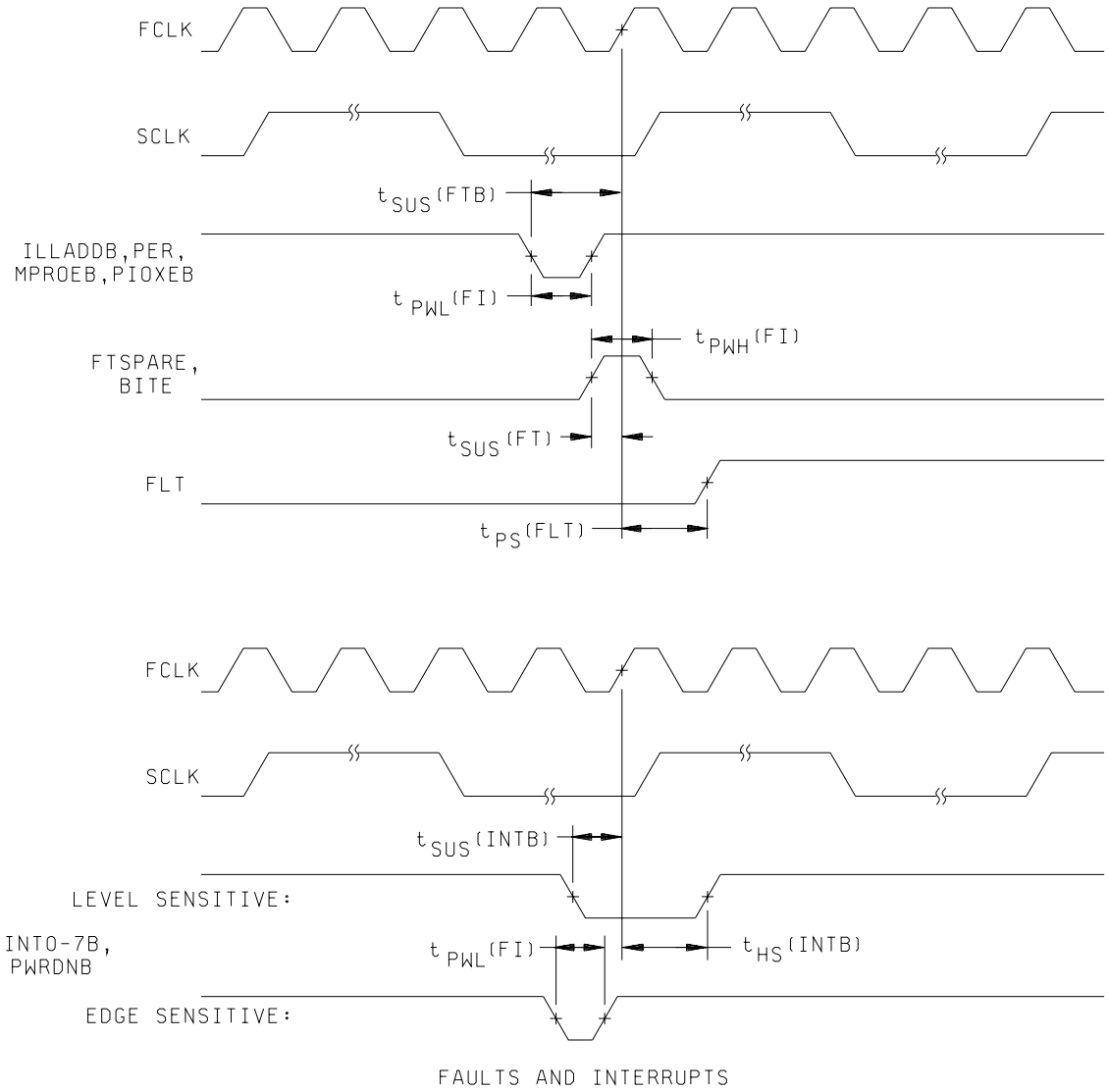


FIGURE 4. Timing waveforms - Continued.

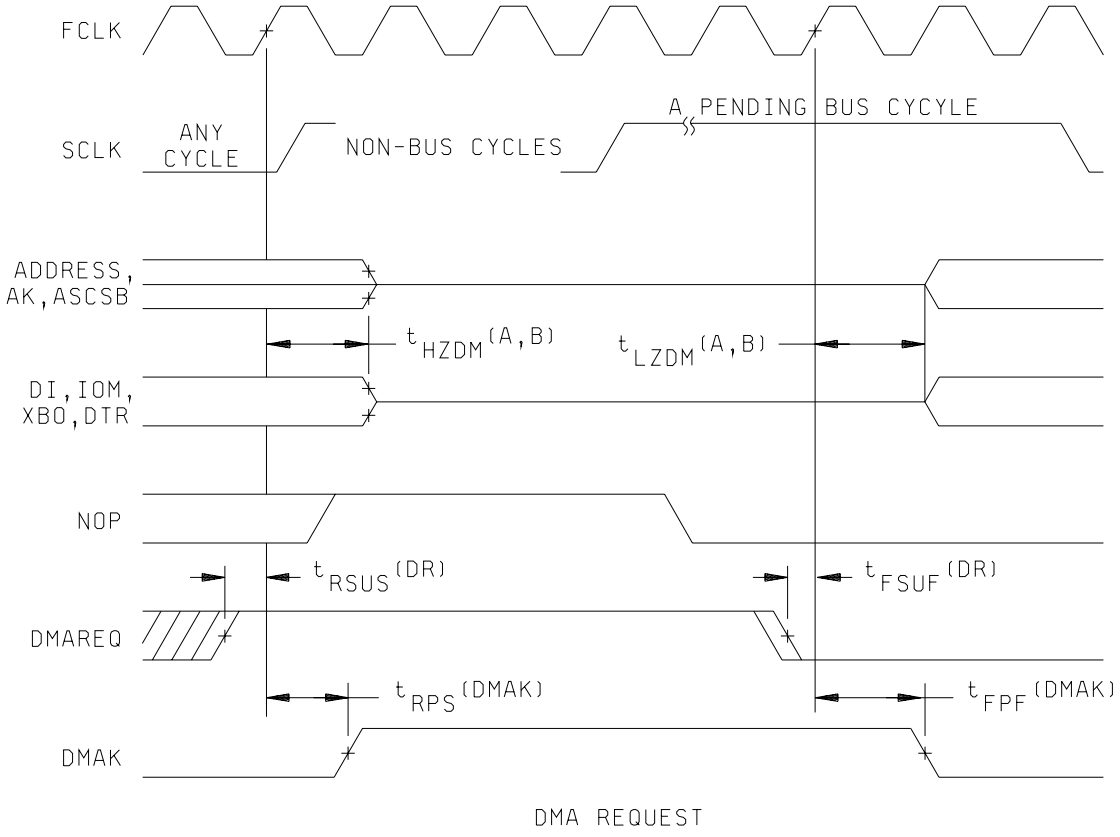


FIGURE 4. Timing waveforms - Continued.

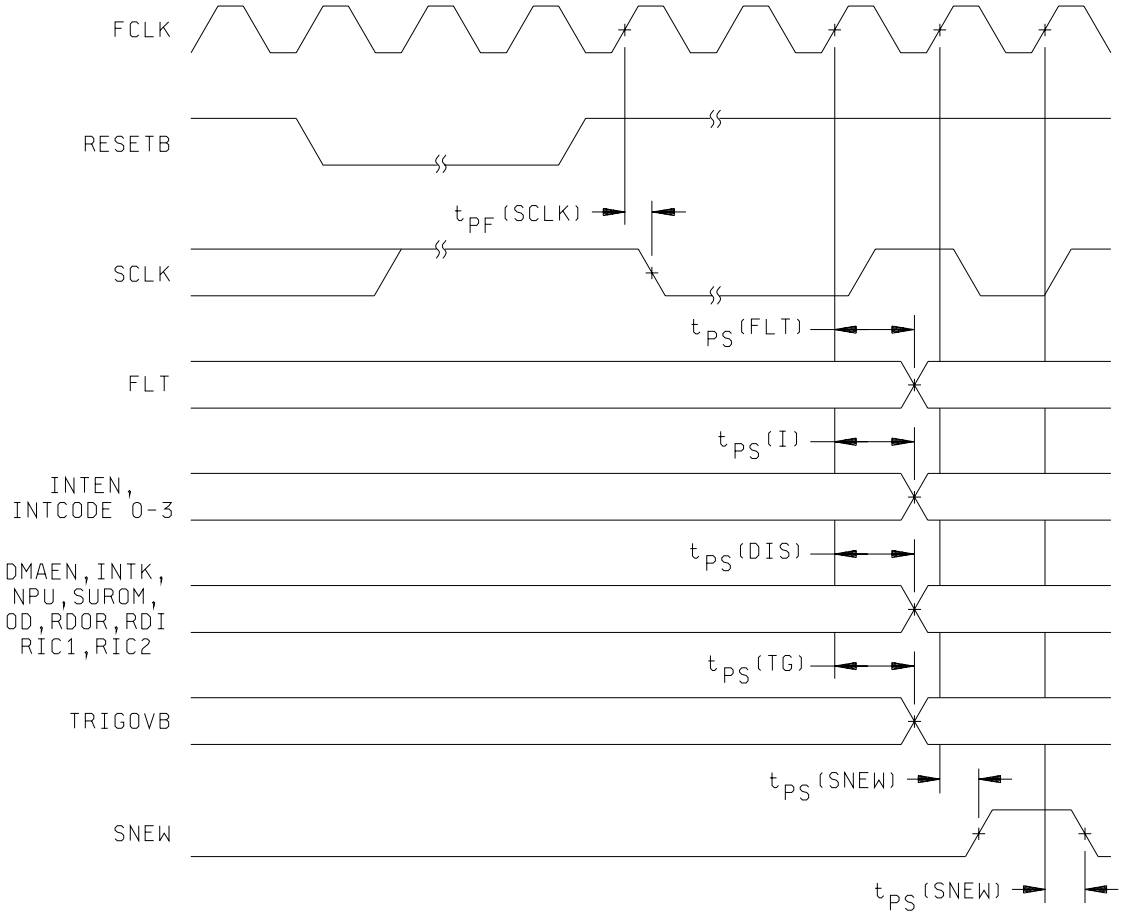
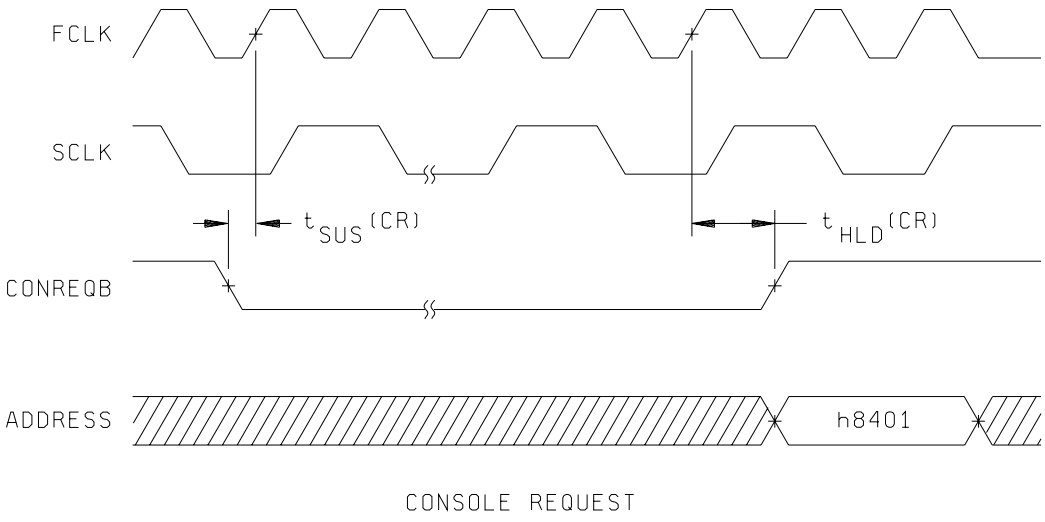
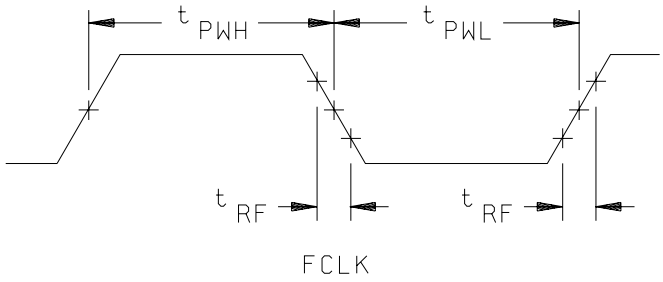


FIGURE 4. Timing waveforms - Continued.



NOTE: t_{HLD}(CR) is referenced to the specific FCLK which generates the SCLK of address = 8401H.



NOTE: All timing measurements are made at the 50% point on waveforms. Exceptions: (1) High impedance delays are measured to the point at which the target signal changes by Vx (Vx = 0.25 V). (2) Rise and fall times are specified from the 10% to 90% points.

FIGURE 4. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 7 and 8 functional testing shall include instruction verification test. These tests form a part of the manufacturer's test tape and shall be maintained and available from approved sources of supply.

d. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. One pin of each input/output driver (buffer) type shall be tested on each sample device. A minimum sample size of five (5) devices with zero (0) failures shall be required.

e. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---		1, 7
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Pin descriptions. The pin descriptions are as defined in table III.

TABLE III. Pin descriptions.

Symbol	Definition	Functional description
V_{SS1-2}	Ground	Electrical ground
V_{DD1-2}	Power	Power supply
A0-A15	Address bus	This output bus provides the logical address for bus transactions and is in a high impedance state when any of the following signals are asserted: RESETB, TSB, DMAK, or NOP. A0 is the most significant bit. High level = 1.
D0-D15	Data bus	This bidirectional bus provides data for transfers to or from external devices and is in a high impedance state when any of the following signals are asserted: RESETB, TSB, DMAK, or NOP. D0 is the most significant bit. High level = 1.
ASCSB0-ASCSB3	Address state/chip select	When expanded memory is present, address state is used for memory address mapping, and is taken directly from the AS field (bits 12 - 15) of the status word with a high level = 1. When expanded memory is not present, these lines may be used as active low chip selects in 16K word boundaries and are decoded from the most significant two bits of the logical address. These lines are in a high impedance state when any of the following signals are asserted: RESETB, TSB, DMAK, or NOP.
AK0-AK3	Access key	Access key is used for pass/fail criterion for the access lock and key option when expanded memory is present and is in a high impedance state when any of the following signals are asserted: RESETB, TSB, DMAK, or NOP. The value of this bus is taken directly from the PS field (bits 8 - 12) of the status word. High level = 1.
DTR	Data bus	This output selects the direction, write vs. read for data transmit/transfer: 1 = write (transmit), 0 = read (receive). It is high impedance when RESETB, TSB, or DMAK is active.
STB	STROBE	The falling edge of the strobe output indicates valid address on the address bus. For a read operation (DTR = 0), the rising edge will coincide with the rise of SCLK and indicates the latching of data into the CPU. For a write operation (DTR = 1), the rising edge will occur before the end of the cycle to accommodate typical data hold times and write recovery requirements. It is high impedance when RESETB is active.
IOM	IO/memory	This output selects between memory and input/output for the current bus cycle; 1 = I/O, 0 = memory. It is high impedance when RESETB, TSB, or DMAK is active.
DI	Data/instruction	This output selects between data (operand) and instruction space for memory accesses; 0 = instruction, 1 = data. It is high impedance when RESETB, TSB, or DMAK is active.
XBO	Extended bus operation	This output is used to recognize certain bus operations including NOP. It is high impedance when RESETB, TSB, or DMAK is active
TSB	Tri state control	When SCANEN = 0, asserting this input places the address bus, data bus, ASCSB0-3, AK0-3, XBO, DI, IOM, and DTR into a high impedance state. Low = assertion. When SCANEN = 1, this input controls the micro-program counter. Low = increment.
DMAREQ	DMA request	DMA request is an input that is used by external DMA devices to request the common bus. High = assertion.
DMAEN	DMA enable	DMA enable is an output that enables external DMA devices allowing them to request the common bus. This signal is controlled by XIO commands DMAE and DMAD. High = assertion.
DMAK	DMA acknowledge	This output is generated in response to a DMA request if DMA is enabled. When this processor grants the common bus to the requesting DMA device, it places the address bus, data bus, ASCSB0-3, AK0-3, DTR, DI, IOM, and XBO lines into a high impedance state, and asserts DMAK relinquishing the bus to the external DMA device. It is high impedance when RESETB is active. High = assertion.

TABLE III. Pin descriptions - Continued.

Symbol	Definition	Functional description
WCODE0 - 4	Wait state code	The wait code inputs specify bus timing for instruction memory, operand memory, and input/output bus. High = 1.
RDY	Bus ready	The RDY input is used for asynchronous bus transfers and indicates when a transfer has completed. High = assertion.
INTEN	Interrupt enable	This output indicates whether interrupts are enabled and is controlled by XIO commands ENBL and DSBL. High = assertion.
INTK	Interrupt acknowledge	This output indicates that an external interrupt has been recognized and latched into the pending interrupt register. High = assertion.
INTKCODE	Interrupt code 0-3	This four bit output indicates which external interrupt level is being acknowledged. Bit 3 is most significant. High = 1.
INT0B - INT7B	External interrupt	these inputs provide the means for external devices to interrupt this processor. INT0 through INT7 are assigned to 1750A interrupt levels 2, 8, and 10 - 15, respectively. Low = assertion.
PWRDNB	Power down	This input indicates the occurrence of a power failure and, when asserted, causes a 1750A level 0 interrupt. Low = assertion.
FTSPARE	Spare fault	This input is a user-definable fault that is assigned to bit seven of the fault register (FT7). Edge sensitive, High = assertion.
PIOXEB	Transmission error fault	This input indicates the occurrence of a transmission error while performing a programmed I/O transfer and is assigned to fault register bit FT6. Edge sensitive, low = assertion.
PEB	Parity error	This input indicates the occurrence of a parity error. When asserted, fault bit FT2, FT3, or FT4 will be set corresponding to memory, PIO, or DMA, respectively. Edge sensitive, low = assertion.
BITE	Built-in test error	This input indicates the occurrence of a built-in test error and causes fault bit FT13 to be set. Edge sensitive, high = assertion.
MPROEB	Memory protect error fault	This input is asserted by the MMU to indicate that an illegal memory access has been attempted. If the attempted transfer was initiated by this processor, fault FT0 is set to 1; if by an external DMA device, fault FT1 is set. Edge sensitive, Low = assertion.
ILLADDB	Illegal address	This input indicates an attempted reference to a memory or I/O location that is not present. If the attempted operation was I/O , fault FT5 is set; if memory, fault FT8 is set. Edge sensitive, low = assertion.
FLT	Fault	This output is the bit-wise 'OR' of the fault register outputs.
CONREQB	Console request	The console request input is asserted by an external maintenance console device. This is sampled at the end of the execution of each instruction and, if active, places the processor in console mode. Low = assertion.
RESETB	System reset	When asserted, this input places the processor in the reset state as defined in table VI of MIL-STD-1750A. The DTR and DMAK are tri-stated. Low = assertion.
SNEW	Start instruction	This output indicates the beginning of the execution phase of a new instruction. High = assertion.

TABLE III. Pin descriptions - Continued.

Symbol	Definition	Functional description
SCANEN	Scan enable	This input activates scan path operation. High = assertion.
SCLK	System clock	This output is the system clock generated in this processor and may be used for synchronization with external hardware.
FCLK	Fast clock	FCLK is the primary timing source for this processor.
SCALE	Clock scale	Relationship between FCLK and SCLK with no wait states; 0 = SCLK period is 4 FCLK periods, 1 = SCLK period is 2 FCLK periods.
TCLK	Timer clock	TCLK is the time base for the timers TA, TB. Nominal frequency is 1.0 MHz.
TGOCLK	Trigger go clock	TGOCLK is the time base for the trigger go counter.
RDI	Discrete input	RDI is an output that is generated by the processor in response to XIO command “Read Discrete Input”. This causes the external discrete input buffer to place its data on the data bus. High = assertion.
OD	Discrete output	OD is an output that is generated by the processor in response to XIO command “Output Discretes”. This causes the external discrete output register to latch the value that is present on the data bus. High = assertion.
RDOR	Read discrete output register	RDOR is an output generated by the processor in response to XIO command “Read Discrete Output Register”. This causes the external discrete output register to place its data on the data bus. High = assertion.
RIC1-RIC2	Read I/O interrupt code	RIC1 and RIC2 are outputs generated by the processor in response to XIO commands “Read I/O Interrupt Code, Level (1 or 2 respectively). This causes the contents of the external level 1 or level 2 IOIC register to be placed on the data bus. High = assertion.
SUROM	Start-up ROM enable	This output is controlled by XIO commands ESUR and DSUR. High = assertion.
NOP	No bus access	This output indicates that no bus access is occurring during the current SCLK cycle (SCANEN = 0), High = assertion. If SCANEN = 1, this output is the scan path data.
NPU	Normal power up	This output reflects the result of the Built-in Test where a high level indicates “Pass”. It may be reset with the XIO command RNS.
TRIGOVB	Trigger GO overflow	This output indicates when the Trigger GO counter has timed out. Low = assertion.
DEFCON	Default configuration	DEFCON is an input that is sampled during reset or break-point and places the device in the default configuration. If inactive, the configuration register is loaded from I/O address 8410H. High = assertion.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-03-05

Approved sources of supply for SMD 5962-05207 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0520701QXC	34168	HX1750XQN
5962-0520701QYC	34168	HX1750YQN
5962-0520701QZC	34168	HX1750ZQN

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell, SSEC 12001 State Highway 55 Plymouth, MN 55441