High Temperature Analog to Digital Converter Reliability Testing

Bruce Ohme and Mark R. Larson
bruce.ohme@honeywell.com
Honeywell Aerospace
Plymouth, Minnesota  USA
Outline / Motivation

HTADC12 - High Temp 12-Bit ADC Reliability Study

• It is common practice to characterize and compensate initial measurement errors in down-hole tools

• Component drift over time and temperature cycling are therefore just as important to know/predict as time-zero accuracy

• Parametric shifts affecting post-compensation accuracy are presented for a 12-bit ADC from samples stressed by 250°C bias plus temperature cycling from -65°C to 200°C

• Mechanical / Assembly data is also presented
HTADC12 Block Diagram

- **12 Bit Successive Approximation ADC**
- **Temperature range:** -55°C to 225°C
- **5V supply:** 0V to VREF full-scale input range
- **On-chip 2.5V Reference**
- **On-chip buffer op amp**
- **4MHz internal clock for conversion**
- **10µs conversion time**
- **Parallel or Serial data outputs**
- **28 or 14 pin DIP package configurations**
Life-test/Temp-Cycle/Test Flowchart

1500 Hours at 250°C + 1000 Temp-cycles (-65°C to 200°C)

Standard Assembly and Screening, Including 44 hr. Burn-in @ 6V, 250°C

23 parts

168 Hrs @ 250°C, 22 Blased 1 Un-powered

23 parts

Test at -55°C, 25C, 225C

23 parts

Continue to 500 Hrs @ 250°C

23 parts

Temperature Cycling
100 cycles
-65°C to +200°C
TM 1010

15 parts

Test at -55°C, 25C, 225C

23 parts

Continue to 1000 Hrs @ 250°C

23 parts

Test at -55°C, 25C, 225C

23 parts

Fine / Gross Leak
TM 1014
Cond A1, C1

900 Additional Temp. Cycles

Test at 25°C

23 parts x 9 total iterations

Die Shear Test
TM2019.5 (post de-lidding)

2 parts

Wire Bond Pull Test
TM2011, Cond. D (post de-lidding)

2 parts

Test at 25°C

Temperature Cycling
100 cycles
-65°C to +200°C
TM 1010
Assembly Details

- Ceramic 28-lead DIP package
  - Multi-layer alumina ceramic
  - Kovar lid / Furnace seal
  - Alloy 42 side-brazed leads
  - Gold over nickel surface metalization

- Gold-backed SOI die
  - Die-size = 2.8mm x 2.9mm
  - Aluminum wirebond pads

- Gold-eutectic die bond
  - Gold (1% Si) die attach preform

- Aluminum ultra-sonic wedge bond
  - 1.25 mil aluminum (1.5% Si) wire

14-lead package uses similar materials/flow
Current production uses high-temp. adhesive die-attach
Life-test Fixture

• High-temp. sockets mounted on aluminum rails.
• Wire-wound resistors
• Nickel wire/Fiberglass sheath
• Welded + Soldered connections (95/5 Pb/Sn solder)
Burn-in / Life-test Configuration

- Configured for continuous conversion at Vin=half-scale
- Buffer Amp configured as voltage-follower with Vin=2.5V
- VDD = 6V (operating = 5V)
- Oven at 250°C
Electrical Test Parameters

- At each electrical test point collected data using automated tester
- On-chip temperature monitored by forward drop of ESD diodes
- Test program collects DC data:
  - Buffer Amplifier offset voltage at 2.5V VIN
  - ADC offset, full-scale, and linearity errors
  - Conversion Time: Controlled by on-chip R-C oscillator
  - No-load output of the 2.5V reference

  Conversion time and VREF tempco/scale-factor are trimmed at wafer test

**Note:**
- The ADC has superior INL/DNL performance at high temp relative to room temperature
- Cross-over from 1.1 to 2.0 LSB INL to 0.5 LSB INL is observed at ≈160°C
- This is attributed to design attributes rather than process/device stability

225°C results provide best insight into performance and stability of the technology
Life-test results (225°C data)

ADC Full-scale Error (Independent of VREF) at 225°C

Full-Scale Drift/Spread over life-test:
Average = 0.016% of FS (0.26 LSB’s)
Worst case = 0.027% of FS (0.44 LSB’s)

ADC Offset Error at 225°C

Offset Drift/Spread over life-test:
Average = 0.55 LSB’s
Worst case = 1.30 LSB’s

- These results are obtained with an external reference applied (i.e., independent of any VREF drift)
- General trend:
  - Full-scale/Offset errors show an initial shift (within 168 hrs) in opposite directions
  - Indicative of an “end-point shift” in the transfer function
Buffered 2.5V reference is generally applied as the ADC Reference Input and defines the full-scale input range

Buffer amplifier may be used to drive the ADC input
  - In that case shift in buffer amplifier offset adds to ADC offset
Temp. Cycling Results (25°C Data)

- Above charts compare data prior to T-cycling (blue) to data obtained after T-cycling (Red)
- Full-scale/Offset shifts in opposite directions are observed
  - Indicative of an “end-point shift” in the transfer function

Offset Drift/Spread over T-cycles:
Average = 0.85 LSB’s
Worst case = 0.87 LSB’s

Full-Scale Drift/Spread over T-cycles:
Average = 0.016% of FS (0.41 LSB’s)
Worst case = 0.027% of FS (0.59 LSB’s)
Integral Non-Linearity (INL) Results

**INL Drift/Spread over life-test:**
Average = 0.04 LSB’s
Worst case = 0.09 LSB’s

- 1500 hours at 250°C + 1000 T-cycles does not significantly change linearity
# Electrical Parameter Summary

## Predicted Accuracy Degradation from Results

<table>
<thead>
<tr>
<th>Source</th>
<th>Typical</th>
<th>Worst-case</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Drift after 1500 hrs @ 250°C</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC Offset and Full-scale</td>
<td>0.81</td>
<td>1.74</td>
<td>LSB's</td>
</tr>
<tr>
<td>Buffer Amplifier</td>
<td>0.36</td>
<td>0.74</td>
<td>LSB's</td>
</tr>
<tr>
<td>VREF</td>
<td>3.1</td>
<td>4.6</td>
<td>LSB's</td>
</tr>
<tr>
<td><strong>Additional Drift from 1000 T-Cycles</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC Offset and Full-scale</td>
<td>1.26</td>
<td>1.46</td>
<td>LSB's</td>
</tr>
<tr>
<td><strong>Total from above sources</strong></td>
<td>5.53</td>
<td>8.54</td>
<td>LSB's % of FS</td>
</tr>
<tr>
<td></td>
<td>0.14</td>
<td>0.21</td>
<td></td>
</tr>
</tbody>
</table>

- Reference drift is dominant error source
- Followed by ADC Offset/Full-scale drift with temperature cycling
- Resolution/Linearity is not significantly impacted
Mechanical / Assembly Test Results

- All parts passed hermeticity tests
  - Mil-Std 883, TM1014, conditions A1, C1
  - 1500 Hours at 250°C, 100 Temperature Cycles (-65°C, 200°C)

- Wire-bond pull tests passed
  - Mil-Std 883, TM1011, condition D
  - 1500 hrs @ 250°C, 1000 T-cycles
  - 2 packages, 70 wires pulled
  - Ave. pull-strength = 5.7 grams, Minimum = 4.9 grams
  - Pass criteria is 2.0 grams

- Die-shear tests passed
  - Mil-Std 883, TM1019
  - 2-die tested : 23.3 kgf / 30.2 kgf shear strength
  - Pass criteria is 1.0 kgf
Summary and Conclusion

• Testing has been completed to provide benchmark data/results for predicting ADC performance over time at high temp. with temperature cycling
• Mechanical integrity, functionality, and linearity are stable over the test conditions
  – 1500 Hours at 250°C, 1000 Temperature Cycles (-65°C, 200°C)
• Total compensated accuracy degradation is 5.5 LSB’s typical (3.3mV for a 2.5V full-scale range)
  – Dominated by reference voltage drift
• Potential for marginal improvement from extended burn-in/pre-conditioning

Honeywell High Temperature Website

www.hightempsolutions.com

Bruce Ohme
bruce.ohme@honeywell.com
Plymouth, Minnesota   USA