Single Package Re-Configurable Processor for Data Acquisition at 250°C

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Abstract

A high-temperature data processing device is required for applications gathering sensor data and control of electronics in environments which operate above 200°C. This paper discusses the process of leveraging advances in high temperature electronics and integrating them for new applications and improved system performance. It centers on the development of the 250°C High Temperature (HT) SOI CMOS process technology, several new HT products, and HT package technology. Honeywell integrates a HT FPGA, SRAM and EEPROM into a Multi-Chip Module (MCM) creating a flexible, re-configurable computing platform for sensor data processing and control applications at 250°C. A reconfigurable processor enables the ability to gather information from multiple sources and then control multiple devices with a single electronics assembly while reducing size, weight and power. Packaged in a small 2.2 x 0.75 inch (56 x 18 mm) MCM, the module operates at clock rates up to 10MHz from a single 5V supply. Although power consumption is strongly dependent on configuration, the targeted demonstration configuration clocked at 1MHz power dissipation is on the order of 100mW. The combination of all these technologies and application code to operate the module provides a significant improvement over existing technology for data acquisition applications.

1. Introduction

Due to the need for High Temperature (HT) electronics, small size and ability to survive in very rugged environments, a module integrating several key data processing components is being presented. Starting from a base high temperature SOI CMOS technology, key electronic functions are developed and then integrated. Each of these are addressed individually and then directed towards a multi-channel data logging application. The MCM design and manufacturing provide long life at high temperatures (250°C) and high reliability in extremely harsh environments.

This MCM is referred to as the Reconfigurable Processor for Data Acquisition (RPDA). Its use is illustrated in a sensor data conversion application referred to as a Multi-Channel Data Acquisition Controller (MCDAC).

2. HT SOI CMOS Technology

The Integrated Grcuits (ICs) are manufactured on 0.8um Silicon On Insulator (SOI) CMOS technology. SOI CMOS has a number of features which allow for electronics to operate at temperatures at and above 250°C.

- Lower Leakage Current – The full oxide isolation SOI technology minimizes junction size and the leakage current which doubles every 10°C (above ≈170°C). The design of the transistors also re-targets transistor threshold voltage implants to reduce leakage.

- Lifetime Extension at High Temp – Electromigration increases at high temperatures and so the IC design and layout rules lower the current densities increasing reliability and lifetime.

3. Package Design and Assembly

High-reliability, high-temperature packaging is an essential element of high temperature systems. The integrated circuits are packaged in a co-fired ceramic Multi-Chip Module (MCM) which provides stable performance at temperatures greater than 250°C. The RPDA MCM has 147 pins (through-hole) to withstand high shock and vibration environments and also contains ceramic chip capacitors.

Proven materials and processes include:

- Package Type: High Temperature Co-fired Ceramic MCM
- External Metal (Plating): Gold over Nickel
- Die Attach: Adhesives and bonding materials to 300°C
- Wirebond: Aluminum
- Hermetic Seal: Welded Kovar Lid

4. Reconfigurable Processor for Data Acquisition (RPDA) Description

Three ICs are integrated into the 147 pin package to implement the RPDA.

- The HTFPGA has equivalent capacity to an Atmel AT6010 component. This provides up to 6400 register elements and/or up to 32,000 equivalent gates of logic. The number of useable gates is dependent upon the application, complexity of the signal routing, and the synthesis process (i.e., the process by which a behavioral design is translated into a gate-level structural design).
- The HTEEPROM has 256Kbits (32k x 8) of total capacity. It is intended to store configuration data that is used to program the HTFPGA and still have space available for non-volatile data storage. Internal voltages of +/-8.5V are used to write memory. The EEPROM can be accessed directly from the module pins with a parallel or serial SPI interface.

  The parallel pins are internally shared with the FPGA, so applications that require loading data into the EEPROM will need to do this while the FPGA signals are in high impedance state.
- The HT6256 SRAM has 256Kbits (32k x 8) of total capacity. The static random-access memory is asynchronous and used for application data memory.
- The small 2.2 x 0.75 inch (56 x 18 mm) HT MCM package technology is an essential element of high temperature electronic systems. Co-fired ceramic Multi-Chip Modules (MCM's) can meet this need with stable performance at temperatures greater than 250°C.

The basic interconnect diagram is shown in Figure 1. The diagram shows access to the interface of the individual ICs. This combined with the programmable I/O of the FPGA delivers the capability to expand the function of the RPDA to control additional devices, add more SRAM or EEPROM or even interface multiple RPDAs.

The proposed RPDA assembly is shown in Figure 2.

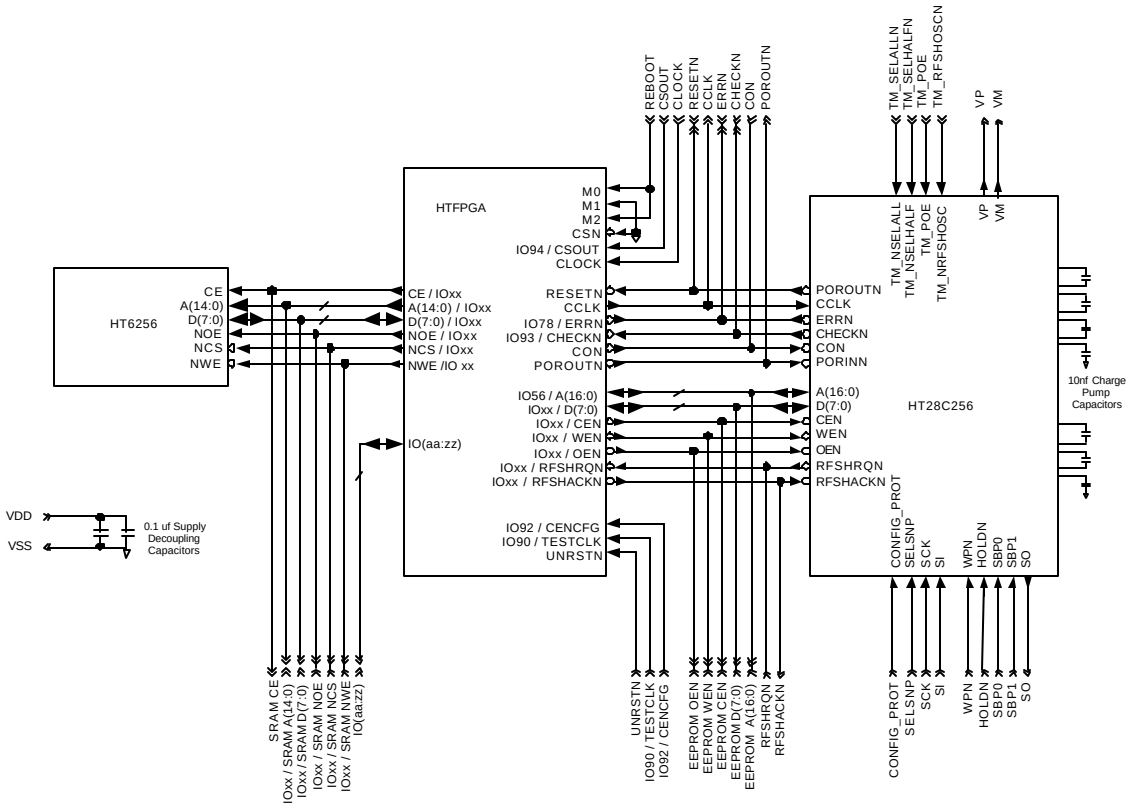


Figure 1 – RPDA Interconnect Diagram

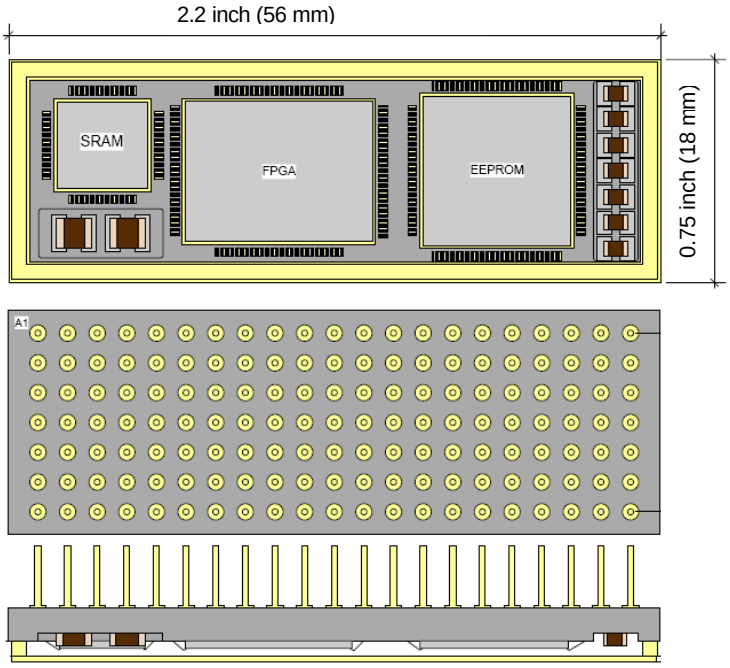


Figure 2 –Hermetic High Temperature RPDA Package, 147 Pin

The FPGA is the central controller and primary interface for data acquisition applications. With the flexibility of re-configurable logic and IO, the FPGA can be adapted to a wide variety of purposes. The RPDA has up to 115 programmable IO (54 configurable IO, 57 shared IO with direct access to SRAM/EEPROM bus) that can be configured by user.

Upon power up, the FPGA is loaded with the configuration data stored in the EEPROM. Loading the configuration data into the EEPROM can be accomplished using a dedicated serial peripheral interface (SPI) bus which is independent of the FPGA, or through the parallel bus which is common with the FPGA.

The SRAM is tightly coupled to the FPGA allowing for use as short term memory applications within the RPDA.

5. Typical Specifications

Parameter	Value
Supply Voltage	5V
Primary Clock	1 MHz
Core Data Rate	100 kHz
Sampling Period	2 sec
Data Download Rate	100 kbps
Operating Current (estimated)	20 mA
Power (Estimated)	100 mW

6. Design and Verification Tools

The RPDA MCM was designed and verified using a number of different development tools. High level simulations were performed to verify interconnect and performance of the three ICs as well as design verification of the FPGA code.

Verification simulations included:

- HTFPGA has been simulated at the logic-gate level.
  - Min/max timing parameters used in simulation
  - RPDA RTL simulations have been performed
  - Exercised HTFPGA/EEPROM and HTFPGA/SRAM interfaces
- MCDAC functional simulations have been performed
  - Exercised HTFPGA/EEPROM/SRAM using test bench
  - Simulations completed post-route HTFPGA timing files
- In addition to the gate-level structural simulations, Register-transfer-level (RTL) simulations were performed at the top-level of the RPDA to verify correct connectivity between the HTFPGA / HTEEPROM and the HTFPGA / HT6256 SRAM.

Schematic Capture and Simulation Tools

- Mentor DA en2002 – schematic capture
- QSimPro 2004SP5 - HTFPGA Quickpart Simulations
- Modelsim 5.8d – HTFPGA Quickpart Simulations
- Modelsim 6.1e – HTFPGA/RPDA HDL Simulations

Logic Synthesis and Routing Tools

- Mentor LeonardoSpectrum 2006b.12 – synthesis
- Atmel Figaro version IDS7.6.7 – P&R
  - Patch level 3 applied (RHrFPGA)
  - HT patch installed (AT6010HLV-010QM)

7. Test Plan

The RPDA test plan includes verification at several levels. The individual die are tested at the wafer level prior to the sawing process. This will include a combination of DC characteristics and functional testing. Once assembled into the MCM, further testing on the DC characteristics and higher level functional test program will take place to verify the interconnect and overall performance. Test vectors generated during the design verification will be used for the functional testing. As part of the product screening, the MCM would be burned in at a temperature of 250°C.

8. RPDA Operation and MCDAC Application

In the MCDAC application, the MCM is configured to control an eight channel analog mux and an 18-bit analog-to-digital converter. The HTEEPROM is only used as a boot ROM which contains the programming for the HTFPGA. The HTSRAM is used as data storage space in the form of an 8K by 32-bit FIFO. The MCDAC can be programmed through external pin selection to perform autonomous measurements of 1 to 8 channels of analog data on a pre-defined schedule. It may also be requested to make asynchronous reads of the ADC by providing signals to the SAMPLE NOW pin and providing a CHAN SELECT address. Control of the device and

unloading the sampled data is stored in the FIFO is through the slave serial port interface (SPI).

The FPGA will be designed to include a main Controller/State Machine. When operating autonomously, it controls the analog mux and will request data and status from the ADC. It then will place the data in memory and prepare it for transmission back to the SPI slave device. All other requests from the SPI Slave block will be handled by the Controller. A typical state diagram is shown in Figure 3.

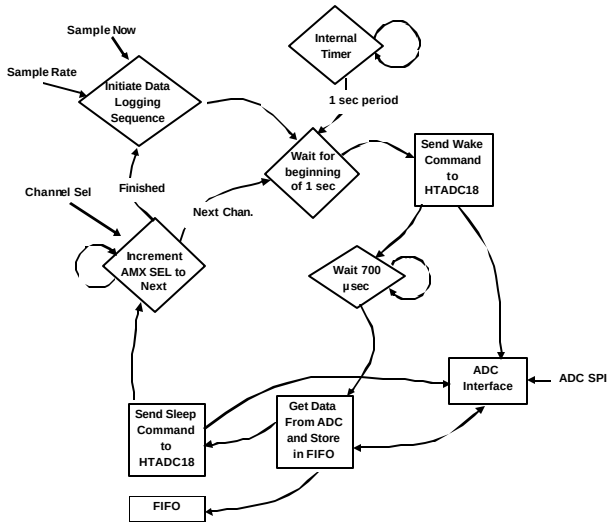
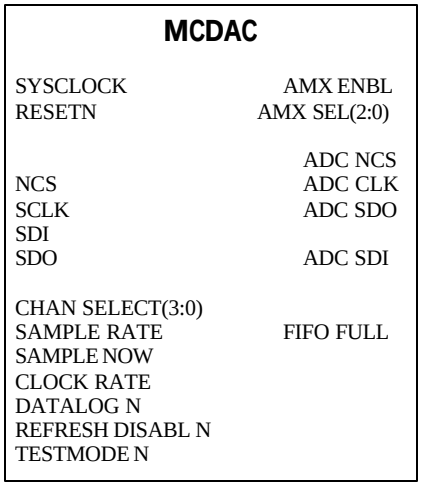


Figure 3 – Typical State Diagram

The SRAM R/W block will access the SRAM's data, address and control ports. It will provide the controller with temporary memory for storing data and status that has been collected from the ADC. Each 18-bit measurement will be stored along with health and status information into a 32-bit word. Up to 8192 32-bit words (8k x 32) can be logged by the on-chip memory. The SPI interface is used for data transfer to and from the MCDAC at data rates up to 1MHz. The SPI bus is activated through a chip select, enabling communication via the SPI Data In and SPI Data Out pins. The FIFO data can be downloaded sequentially, or most recent measurement data can be downloaded.

The functional RPDA signals used for the MCDAC application are shown Figure 4.



Signal	Type	Function
SYSCLOCK	IN	1MHz Module Clock
RESETN	IN	Global Reset
ADC_NCS	OUT	ADC SPI Chip Select
ADC_CLK	OUT	ADC SPI Clock
ADC_SDO	OUT	ADC SPI Serial Data Out
ADC_SDI	IN	ADC SPI Data In
NCS	IN	SPI Slave Chip Select
SCLK	IN	SPI Slave Clock
SDO	OUT	SPI Slave Serial Data Out
SDI	IN	SPI Slave Data In
CHANNEL_SEL(3:0)	IN	Analog Channel Select
SAMPLE_RATE(1:0)	IN	Autonomous Sample Rate
SAMPLE_NOW	IN	External Sample
DATALOG_N	IN	Enable/Disable FIFO
AMX_ENA	OUT	Analog MUX Enable
AMX_SEL(2:0)	OUT	Analog Mux Select Bus
FIFO_FULL	OUT	FIFO Full Indicator
REFRESH_DISABL_N	IN	Enbl/Disbl EEPROM
CLOCK_RATE	IN	SYSCLK Rate (1=1MHz,
TESTMODE_N	IN	Manufacturing Test Signal

Figure 4 – RPDA Symbol And Signal Definition For MCDAC Application

A functional block diagram of the MCDAC application is shown in Figure 5.

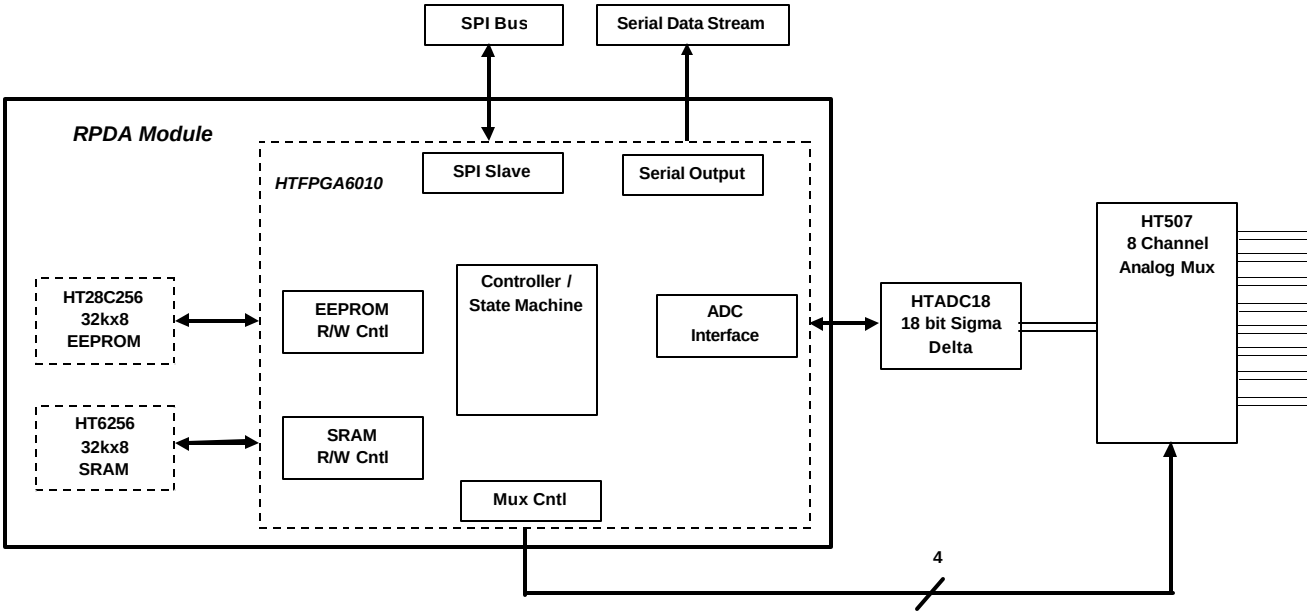


Figure 5 - Multi Channel Data Acquisition Application

9. Summary and Conclusions

In order to fulfill the need for data logging and control applications at extreme temperatures, an electronics module leveraging advances in high temperature SOI CMOS, circuit design and packaging has been defined. The combination of technologies and integration of an FPGA, EEPROM, and SRAM in the RPDA has created a flexible, re-configurable data processor. Packaged in a rugged multi-chip module provides size and power reduction allowing electronics to be installed in small spaces with temperature extremes greater than 250°C such as engines and down-hole drilling applications.

With access to the interface of the ICs, easy expansion for many applications is attained.

10. References

1. Honeywell "*Reconfigurable Processor for Data Acquisition (RPDA) Data Acquisition System Objectives Specification*" Rev 1.0, dated 12 October 2007.
2. Honeywell "*HTADC18 High Temperature 18-bit Differential Input S? ADC with Built-in Clock, Voltage Reference and SPI Interface*" Datasheet dated 9-15-2006
3. Honeywell *"HT506/507 High Temperature Analog Multiplexers 16-Channel Single / 8-Channel Dual*" Datasheet – 4/98.
4. Atmel *"Coprocessor Field Programmable Gate Arrays AT6000(LV) Series"* dated 10/99
5. Atmel *"Field Programmable Gate Array Configuration Guide"* for AT6000 Series Devices, dated 9/99

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