REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47							
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

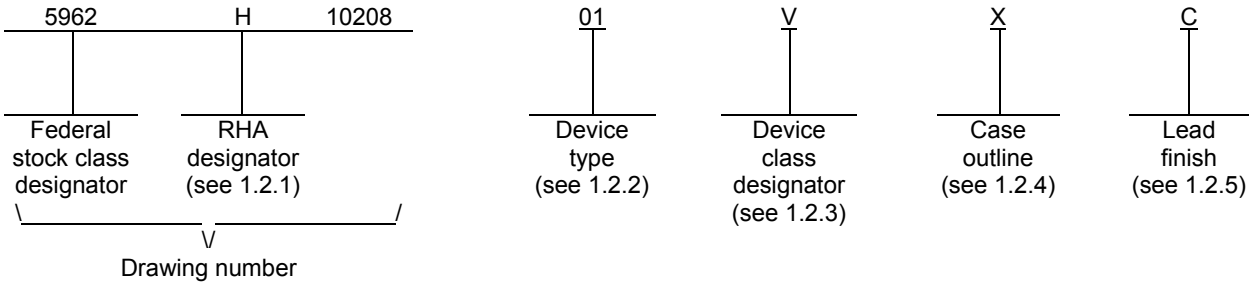
REV STATUS	REV															
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A	PREPARED BY Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Phu H. Nguyen APPROVED BY Thomas M. Hess DRAWING APPROVAL DATE 10-09-01 REVISION LEVEL	MICROCIRCUIT, DIGITAL, ASIC, RADIATION HARDENED, SOI CMOS, SERIALIZER/DESERIALIZER (SERDES), MONOLITHIC SILICON SIZE A | CAGE CODE **67268** | **5962-10208** SHEET 1 OF 47

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HXSRD01T(Q or V)H	Quad Redundant SERDES

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	468	Land Grid Array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Core supply voltage range. (V_{DD}) ..... -0.5V to +2.5 V
SSTL-2 Supply voltage, (V_{DD2}) ..... -0.5 V to +4.6 V
Input voltage ..... -0.5 V to V_{DDx} + 0.5 V 2/ 3/
Output voltage ..... -0.5 V to V_{DDX} + 0.5 V 2/ 3/
Maximum junction temperature ..... +175°C
Thermal resistance, junction to case, (θ_{JC}) ..... 1.36 °C/W
Storage temperature range. (T_{STG}) ..... -65°C to +150°C
ESD – HBM ..... Class 1C
Typical power dissipation 4/

Trivor Configuration 5/ 6/ 7/ 8/ 9/	1.0625 Gbps (mW)	2.125 Gbps (mW)	3.125 Gbps (mW)	3.1875 Gbps (mW)
CMU only 10/	221	306	410	425
Single port 11/	1087	1363	1766	1786
Single Lane 12/ 17/	535	675	902	907
Single Transmit Port 13/	484	612	806	810
Single Transmit Lane 14/ 17/	383	488	662	664
Single Receive Port 15/	826	1057	1370	1400
Single Receive Lane 16/	373	493	650	668

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability
2/ V_{DDx} (relevant supply) must be at recommended DC level. When V_{DDx} is above recommended levels then absolute limits for inputs and outputs are capped by the limit for V_{DDx}.
3/ Absolute maximum levels for cold spare I/O when V_{DDx} is 0V are the same as the limit for the relevant V_{DDx}.
4/ The power varies depending on the device configuration. Values below include the following test configuration settings:
- Serial transmitter output amplitude : 1600 mV
- PLL Divider setting: Div 10
- Line rate setting: Set as necessary to achieve proper data rate
- Nominal/Default settings for: VDD, VDDA, Pre-Emphasis and equalization.

5/ SSTL-2 power is not included because it consumes power from the 2.5 V supply.
6/ SSTL-2 power estimate is 450 mW per port or 112.5 mW per lane.
7/ Power number are based on transmitting and receiving the CJTPAT.
8/ The 1.8 V power consumptions includes the VDD and VDDA supply power which provides power to the SERDES macro and Trivor logic that is external to the SERDES macro. All SERDES and Trivor Logic is included in this estimate.
9/ These are typical values and are not tested on a part-by-part basis.
10/ CMU power includes the PLL and associated clock trees in Trivor and SERDES8_TOP.
11/ Full port power includes both transmit and receive channels for 4 lanes and the CMU power.
12/ Full lane power includes both transmit and receive channels for 1 lane and the CMU power.
13/ Transmit port power includes only the transmit channels for 4 lanes and the CMU power.
14/ Transmit lane power includes only the transmit channels for 1 lane and the CMU power.
15/ Receive port power includes only the receive channels for 4 lanes and the CMU power.
16/ Receive lane power includes only the receive channels for 1 lane and the CMU power.
17/ The average power per transmit lane decreases as additional lanes are utilized within a port due to port level clock distribution overhead.

1.4 Recommended operating conditions.

DC supply voltage range. (V_{DD})	+1.71 V to +1.89 V
DC supply voltage range. (V_{DD2})	+2.3 V to +2.7 V
CMOS input signal voltage	-0.3 V to V_{DDx} + 0.3 V
CMOS output signal voltage	-0.3 V to V_{DDx} + 0.3 V
LVPECL DC input signal voltage	-0.13 V to V_{DDx} + 0.3 V 18/
LVPECL differential input voltage	+ 100 mV to V_{DD} 19/
LVPECL DC common mode voltage	20/
Case temperature	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	95.49 percent

1.6 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	≥1E6 Rads(Si)
Heavy Ion Single event upset rate (Adam's 10% worst case environment)	$<1x10^{-12}$ Data Bit Errors/Bits Sent 21/
Proton Single event upset rate (Adam's 10% worst case environment)	$<2x10^{-12}$ Data Bit Errors/Bits Sent 21/
Neutron irradiation	≥1E14 neutrons/cm^2 22/
Dose rate data upset	≥1E10 Rad(Si)/sec for < 50 nsec
Dose rate survivability	1E12 Rad(Si)/sec for < 50 nsec
Latchup	Immune by SOI technology.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

18/ This specifies the maximum allowable DC delta between the two inputs
19/ This specifies the minimum input differential voltage required for switching. This differential voltage is ABS(VINP-VINN).
20/ These signals require AC coupling, therefore the Common Mode Voltage requirement is not applicable.
21/ The Bit Error Ratio (BER) is defined as the number of bit errors per bits sent due to ion-induced single event upsets.
22/ Guaranteed but not tested for 1 MeV equivalent neutrons.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, P. O. Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Pin group translation table. The pin group translation table shall be as specified on figure 3.

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.2.6 Burn in circuit. The burn in circuit shall be as specified on figure 6.

3.2.7 SSTL-2 AC timing waveforms. The SSTL-2 AC timing waveforms shall be as specified on figure 7-12.

3.2.8 Functional tests. Various functional tests used to test this device are contained in the figure 7. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. The functional test vectors are listed in figure 7.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $1.71\ V \le V_{DD} \le 1.89\ V$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified 2/ 3/	Group A subgroups	Limits		Unit
				Min	Max	
Input Leakage Current Low, 1.8V CMOS/Schmitt Trigger Inputs with padpull disabled (Pin Group = INPUT_CMOS_PN_18 INPUT_CMOS_PU_PN_18) 4/	I_{IL1_18}	V_{DD} = 1.89 V V_{IN} = 0.0 V	1,2,3	-10	10	µA
Input Leakage Current High, 1.8V CMOS/Schmitt Trigger Inputs with padpull disabled (Pin Group = INPUT_CMOS_PN_18 INPUT_CMOS_PU_PN_18)	I_{IH1_18}	V_{DD} = 1.89 V V_{IN} = 0.0 V	1,2,3	-10	10	µA
Input Leakage Current Low, 1.8V CMOS/Schmitt Trigger Inputs with padpull in pullup mode (Pin Group = INPUT_CMOS_PU_PN_18)	I_{IL2_18}	V_{DD} = 1.89 V V_{IN} = 0.0 V	1,2,3	-407	-116	µA
Input Leakage Current High, 1.8V CMOS/Schmitt Trigger Inputs with padpull in pullup mode (Pin Group = INPUT_CMOS_PU_PN_18)	I_{IH2_18}	V_{DD} = 1.89 V V_{IN} = V_{DD}	1,2,3	-10	10	µA
Input Leakage Current Low, 1.8V CMOS/Schmitt Trigger Inputs with padpull in pulldown mode (Pin Group = INPUT_CMOS_PD_PN_18)	I_{IL3_18}	V_{DD} = 1.89 V V_{IN} = 0.0 V	1,2,3	-10	10	µA
Input Leakage Current High, 1.8V CMOS/Schmitt Trigger Inputs with padpull in pulldown mode (Pin Group = INPUT_CMOS_PD_PN_18) 4/	I_{IH3_18}	V_{DD} = 1.89 V V_{IN} = V_{DD}	1,2,3	116	407	µA
Tri-State Leakage Current Low, 1.8V CMOS/Schmitt Trigger tri-state outputs and bidirectionals with padpull in pulldown mode (Pin Group = TRI_BI_CMOS_PG_18, TRI_BI_CMOS_RL_PN_18) (Test Vector = see Figure 7) 5/	I_{OZL4_18}	V_{DD} = 1.71 V V_{OUT} = 0.4 V	1,2,3	31	186	µA
Tri-State Leakage Current High, 1.8V CMOS/Schmitt Trigger tri-state outputs and bidirectionals with padpull in pulldown mode (Pin Group = TRI_BI_CMOS_PG_18, TRI_BI_CMOS_RL_PN_18) (Test Vector = see Figure 7) 5/	I_{OZH4_18}	V_{DD} = 1.71V V_{OUT} = 1.31V	1,2,3	-186	-31	µA
Tri-State Leakage Current Low, Voltage Reference Output SSTL-2 (Pin Group = OUT_SSTL_REF_25) (Test Vector = see Figure 7)	I_{OZL3_T25}	V_{DD} = 1.89V V_{DD2} = 2.70V V_{OUT} = 0.0V	1,2,3	-680	-170	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $1.71\ V \le V_{DD} \le 1.89\ V$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified 2/ 3/	Group A subgroups	Limits		Unit
				Min	Max	
Tri-State Leakage Current High, Voltage Reference Output SSTL-2 (Pin Group = OUT_SSTL_REF_25) (Test Vector = see Figure 7)	I_{OZH3_T25}	V_{DD} = 1.89V V_{DD2} = 2.70V V_{OUT} = 2.70V	1,2,3	170	680	µA
Voltage Output Low, 1.8V 3 mA CMOS Outputs and bidirectionals (Pin Group = OUT_TRI_BI_CMOS_3MA_18) (Test Vector = see Figure 7)	V_{OL1_18}	V_{DD} = 1.71V V_{DD2} = 2.3V I_{OL} = 3.0 mA	1,2,3		0.43	V
Voltage Output High, 1.8V 3 mA CMOS Outputs and bidirectionals (Pin Group = OUT_TRI_BI_CMOS_3MA_18) (Test Vector = see Figure 7)	V_{OH1_18}	V_{DD} = 1.71V V_{DD2} = 2.3V I_{OH} = -3.0 mA	1,2,3	1.28		V
Voltage Output Low, 1.8V 9 mA CMOS Outputs and bidirectionals (Pin Group = OUT_TRI_BI_CMOS_9MA_18) (Test Vector = see Figure 7)	V_{OL3_18}	V_{DD} = 1.71V V_{DD2} = 2.3V I_{OL} = 9.0 mA	1,2,3		0.43	V
Voltage Output High, 1.8V 9 mA CMOS Outputs and bidirectionals (Pin Group = OUT_TRI_BI_CMOS_9MA_18) (Test Vector = see Figure 7)	V_{OH3_18}	V_{DD} = 1.71V V_{DD2} = 2.3V I_{OH} = -9.0 mA	1,2,3	1.28		V
Input Threshold Voltage Low, 1.8V CMOS Inputs and bidirectionals (Pin Group = INPUT_BI_CMOS_18) (Test Vector = see Figure 7)	V_{IL1_18}	V_{DD} = 1.71V	1,2,3	0.60		V
Input Threshold Voltage High, 1.8V CMOS Inputs and bidirectionals (Pin Group = INPUT_BI_CMOS_18) (Test Vector = see Figure 7)	V_{IH1_18}	V_{DD} = 1.89V	1,2,3		1.23	V
Falling Input Threshold Voltage Schmitt Trigger Inputs and bidirectionals (Pin Group = INPUT_BI_SCHM_18) (Test Vector = see Figure 7)	V_{T-}	V_{DD} = 1.71V	1,2,3	0.51		V
Rising Input Threshold Voltage Schmitt Trigger Inputs and bidirectionals (Pin Group = INPUT_BI_SCHM_18) (Test Vector = see Figure 7)	V_{T+}	V_{DD} = 1.89V	1,2,3		1.32	V
Hysteresis for Schmitt Trigger Inputs and bidirectionals (Pin Group = INPUT_BI_SCHM_18) (Test Vector = see Figure 7)	V_{HYS}	V_{DD} = 1.71V	1,2,3	0.104		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $1.71\ V \le V_{DD} \le 1.89\ V$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified 2/ 3/	Group A subgroups	Limits		Unit
				Min	Max	
Input Leakage Current Low, LVPECL Inputs (Pin Group = INPUT_SERDES_LVPECL_18) 6/	I_{IL1_SP18}	V_{DD} = 1.89V V_{IN} = 0.0V	1,2,3	-10	-10	uA
Input Leakage Current High, LVPECL Inputs (Pin Group = INPUT_SERDES_DIFF_18) 6/	I_{IH1_SH18}	V_{DD} = 1.89V V_{IN} = 1.89V	1,2,3	-10	10	uA
Input Leakage Current Low, LVPECL Inputs (Pin Group = INPUT_SERDES_DIFF_18) 6/	I_{IL1_SH18}	V_{DD} = 1.89V V_{IN} = 0.0V	1,2,3	-10	-10	uA
Input Leakage Current High, LVPECL Inputs (Pin Group = INPUT_SERDES_LVPECL_18) 6/	I_{IH1_SP18}	V_{DD} = 1.89V V_{IN} = 1.89V	1,2,3	-10	10	uA
Differential input voltage for SERDES inputs (Pin Group = INPUT_SERDES_DIFF_18) (Test Vector = see Figure 7)	VID1_SH18	V_{DD} = 1.71V V_{CM} = 0.855V, V_{ID} = 280mV	7, 8	PASS		
Differential input voltage for SERDES inputs (Pin Group = INPUT_SERDES_DIFF_18) (Test Vector = see Figure 7	VID2_SH18	VDD = 1.89V VCM = 0.945V VID = 280mV	7, 8	PASS		
Differential input voltage for SERDES inputs (Pin Group = INPUT_SERDES_LVPECL_18) (Test Vector = see Figure 7)	VID1_SP18_MUL	V_{DD} = 1.71V VCM = 0.855V VID = 300mV Voting Test: Vector is run up to 50 times at up to 6 strobe points and exits on first pass	7, 8	PASS		
Temperature Diode Voltage (Pin Group = INPUT_DIODE)	V_{OL1_D}	V_{DD}= 1.89V, V_{DD2}= 2.7V I_{ANODE} = 100 µA	1,2,3	0.3	1.0	V
Temperature Diode Voltage (Pin Group = INPUT_DIODE)	V_{OL2_D}	V_{DD}= 1.89V , V_{DD2}= 2.7V I_{ANODE} = 6 µA	1,2,3	0.3	1.0	V
Temperature Diode Voltage (Pin Group = INPUT_DIODE)	V_{OL3_D}	V_{DD}= 1.89V , V_{DD2}= 2.7V I_{ANODE} = 36 µA	1,2,3	0.3	1.0	V
Temperature Diode Voltage (Pin Group = INPUT_DIODE)	V_{OL4_D}	V_{DD}= 1.89V , V_{DD2}= 2.7V I_{ANODE} = 96 µA	1,2,3	0.3	1.0	V
Temperature Diode Ideality Factor Calculation 7/	ETA_D					
Temperature Diode Series Resistance Calculation 7/	R_D					

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $1.71\ V \le V_{DD} \le 1.89\ V$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified 2/ 3/	Group A subgroups	Limits		Unit
				Min	Max	
Input Leakage Current Low, SSTL-2 Inputs (Pin Group = INPUT_SSTL_25) 8/	I_{IL1_T25}	V_{DD} = 1.89V, V_{DD2} = 2.7V V_{IN} = 0.0V	1,2,3	-10	10	µA
Input Leakage Current High, SSTL-2 Inputs (Pin Group = INPUT_SSTL_25) 8/	I_{IH1_T25}	V_{DD} = 1.89V, V_{DD2} = 2.7V V_{IN} = VDD2	1,2,3	-10	10	µA
Input Leakage Current High, SSTL-2 Reference Input (Pin Group = IN_SSTL_REF_25) 8/	I_{IH1_T25R}	V_{DD} = 1.89V, V_{DD2} = 2.7V V_{IN} = VDD2*0.5	1,2,3	-10	10	µA
Voltage Output Low Class I SSTL-2 Outputs and bidirectionals (Pin Group = TRI_LO_BI_SSTL_25) (Test Vector = see Figure 7) 9/	V_{OL1_T25}	V_{DD} = 1.71V, V_{DD2} = 2.3V I_{OL} = 8.1 mA	1,2,3		0.76	V
Voltage Output High, Class I SSTL-2 Outputs and bidirectionals (Pin Group = TRI_LO_BI_SSTL_25) (Test Vector = Figure 7) 9/	V_{OH1_T25}	V_{DD} = 1.71V, V_{DD2} = 2.3V I_{OH} = -8.1 mA	1,2,3	1.54		V
Differential input voltage for SSTL 2.5v inputs (Pin Group = INPUT_BI_SSTL_25) (Test Vector = see Figure 7)	VILH1_T25_MUL	V_{DD} = 1.71V, V_{DD2} = 2.3V V_{IN} = VREF +/- 310mV VREF = VDD2*0.49 & VREF = VDD2*0.51 Voting Test: Vector is run up to 50 times at up to 6 strobe points and exits on first pass	7, 8	PASS		
Differential input voltage for SSTL 2.5v inputs (Pin Group = INPUT_BI_SSTL_25) (Test Vector = see Figure 7)	VILH2_T25_MUL	V_{DD} = 1.89V, V_{DD2} = 2.7V V_{IN} = VREF +/- 310mV VREF = VDD2*0.49 & VREF = VDD2*0.51 Voting Test: Vector is run up to 50 times at up to 6 strobe points and exits on first pass	7, 8	PASS		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $1.71\ V \le V_{DD} \le 1.89\ V$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified 2/ 3/	Group A subgroups	Limits		Unit
				Min	Max	
Voltage Reference Output SSTL-2 (Pin Group = OUT_SSTL_REF_25) (Test Vector = see Figure 7)	V_{OH3_T25}	V_{DD} = 1.71V V_{DD2} = 2.3V I_O = 0 mA	1,2,3	1.035	1.265	V
Voltage Reference Output SSTL-2 (Pin Group = OUT_SSTL_REF_25) (Test Vector = see Figure 7)	V_{OH4_T25}	V_{DD} = 1.89V V_{DD2} = 2.7V I_{OH} = 0 mA	1,2,3	1.215	1.485	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD1L_SD18}	V_{DD} = 1.71V	4,5,6	0.22	n/a	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD2L_SD18}	V_{DD} = 1.71V	4,5,6	0.42	n/a	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD3L_SD18}	V_{DD} = 1.71V	4,5,6	0.62	n/a	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD4L_SD18}	V_{DD} = 1.71V	4,5,6	0.82	n/a	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD5L_SD18}	V_{DD} = 1.71V	4,5,6	1.02	n/a	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD6L_SD18}	V_{DD} = 1.71V	4,5,6	1.22	n/a	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $1.71\ V \le V_{DD} \le 1.89\ V$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified 2/ 3/	Group A subgroups	Limits		Unit
				Min	Max	
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD1H_SD18}	V_{DD}= 1.89V	4,5,6	n/a	1.3	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD2H_SD18}	V_{DD}= 1.89V	4,5,6	n/a	1.7	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD3H_SD18}	V_{DD}= 1.89V	4,5,6	n/a	2.1	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD4H_SD18}	V_{DD}= 1.89V	4,5,6	n/a	2.5	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD5H_SD18}	V_{DD}= 1.89V	4,5,6	n/a	2.9	V
Output Voltage Differential 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 10/	V_{OD6H_SD18}	V_{DD}= 1.89V	4,5,6	n/a	3.3	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS1L_SD18}	VDD = 1.71V	4,5,6	0	VDD	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS2L_SD18}	VDD = 1.71V	4,5,6	0	VDD	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS3L_SD18}	VDD = 1.71V	4,5,6	0	VDD	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $1.71\ V \le V_{DD} \le 1.89\ V$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified 2/ 3/	Group A subgroups	Limits		Unit
				Min	Max	
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS4L_SD18}	V_{DD} = 1.71V	4,5,6	0	V_{DD}	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS5L_SD18}	V_{DD} = 1.71V	4,5,6	0	V_{DD}	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS6L_SD18}	V_{DD} = 1.71V	4,5,6	0	V_{DD}	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS1H_SD18}	V_{DD}= 1.89V	4,5,6	0	V_{DD}	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS2H_SD18}	V_{DD}= 1.89V	4,5,6	0	V_{DD}	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS3H_SD18}	V_{DD}= 1.89V	4,5,6	0	VDD	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS4H_SD18}	V_{DD}= 1.89V	4,5,6	0	VDD	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS5H_SD18}	V_{DD}= 1.89V	4,5,6	0	VDD	V
Output Offset Voltage 1.8V SERDES Outputs (Pin Group = OUTPUT_SERDES_DIFF_18) 11/	V_{OS6H_SD18}	V_{DD}= 1.89V	4,5,6	0	VDD	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $1.71\ V \le V_{DD} \le 1.89\ V$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified 2/ 3/	Group A subgroups	Limits		Unit
				Min	Max	
Quiescent Digital Supply Current Buffers in mode with no static current (Test Vector = ATPG_IDDQ_C3) (Stop Points = 3711, 11133, 22266, 25977, 37110, 40821, 51954, 63087, 66798, 70509, 74220, 85353, 89064, 92775) 24/	I_{DDQ_18}	V_{DD} = 1.89V V_{DD2} = 2.7V f_C = 0 MHz	1,2,3		16	mA
Quiescent Analog Supply Current Buffers in mode with no static current (Test Vector = IDDQ_READS) (Stop Point = 29950)	I_{DDQ_18A}	V_{DD} = 1.89V V_{DD2} = 2.7V f_C = 0 MHz	1,2,3		16	mA
Quiescent VDD2 Supply Current Buffers in mode with no static current (Test Vector = IDDQ_READS) (Stop Point = 29950)	I_{DDQ_25}	V_{DD} = 1.89V V_{DD2} = 2.7V f_C = 0 MHz	1,2,3		5	mA
Functional Vector Sets Vector sets = see Figure 7	FUNC	V_{DD2} = 2.3V & 2.7V, V_{DD} = 1.71V & 1.89V, V_{IN} = See Note 12/	7,8	Pass		
SERDES serial input and output specifications 25/						
Differential Input Amplitude	V_{INDIFF} 26/		9, 10, 11	150	VDDA + 0.3	mV p-p
Input leakage current	IIH, IIL			-20	20	µA
Differential Input Common Mode	V_{INCM} 27/			NA		mV
RX total Jitter Tolerance at the high-speed receiver. 1GE	RX_TJ 28/ 29/				0.68	UI
RX total Jitter Tolerance at the high-speed receiver. 10GE					0.65	
RX total Jitter Tolerance at the high-speed receiver. 1GFC					0.68	
RX total Jitter Tolerance at the high-speed receiver. 2GFC					0.62	
RX total Jitter Tolerance at the high-speed receiver. 10GFC					0.65	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $1.71\ V \le V_{DD} \le 1.89\ V$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified 2/ 3/	Group A subgroups	Limits		Unit
				Min	Max	
SERDES serial input and output specifications – Continued 25/						
RX deterministic jitter tolerance at the high-speed receiver. 1GE	RX_DJ 30/		9, 10, 11		0.33	UI
RX deterministic jitter tolerance at the high-speed receiver. 10GE					0.37	
RX deterministic jitter tolerance at the high-speed receiver. 1GFC					0.33	
RX deterministic jitter tolerance at the high-speed receiver. 2GFC					0.37	
RX deterministic jitter tolerance at the high-speed receiver. 10GFC					0.37	
Differential Output Amplitude	$V_{OUTDIFF}$ 26/			600	1600	mVp-p
Differential Output Common Mode	V_{OUTCM} 26/ 28/			0.8	1	V
Differential Output Rise and Fall Time (20% - 80%)	Tr, Tf 28/			90 TYP		ps
Total Jitter on the high-speed transmit output buffer. 1GE.	TX_TJ 28/				0.23	UI
Total Jitter on the high-speed transmit output buffer. 10GE.					0.35	
Total Jitter on the high-speed transmit output buffer. 1GFC					0.23	
Total Jitter on the high-speed transmit output buffer. 2GFC					0.33	
Total Jitter on the high-speed transmit output buffer. 10GFC.					0.35	
Deterministic Jitter on the high-speed transmit output buffer. 1GE	TX_DJ 28/				0.11	UI
Deterministic Jitter on the high-speed transmit output buffer. 10GE					0.17	
Deterministic Jitter on the high-speed transmit output buffer. 1GFC					0.11	
Deterministic Jitter on the high-speed transmit output buffer. 2GFC					0.2	
Deterministic Jitter on the high-speed transmit output buffer. 10GFC					0.17	

See footnote on the next page

TABLE I. Electrical performance characteristics - Continued.

1/ Translation of PIN_GROUPS can be found in Figure 3.

2/ $V_{DDA} = V_{DD}$, unless noted otherwise.

3/ Input voltage levels are as follows, unless noted otherwise:

IN_CMOS_PN_18, IN_CMOS_PU_PN_18, IN_CMOS_PD_PN_18, IN_SCHM_PN_18,
BI_CMOS_PG_9MA_18: V_{IN} = 0.0V or VDD
IN_SERDES_LVPECL_18: V_{IN} = (VDD * 0.25) or (VDD * 0.75)
IN_SERDES_DIFF_18: V_{IN} = (VDD * 0.25) or (VDD * 0.75)
IN_SSTL_T_25: V_{IN} = (VDD2 * 0.5 – 0.6V) or (VDD2 * 0.5 + 0.6V)
IN_SSTL_REF_25: V_{IN} = 0.25V or VDD2 * 0.5

RHA parts for device type 01 supplied to this drawing have been designed and tested to level “H”. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25□C.

4/ Pin IDDQPIN (H17) is not tested for IIL1_18 or IIH3_18, since it controls the state of its own programmable pad pull condition.

5/ Signal MDIO (pin V4) cannot be tested for IOZL4_18 or IOZH4_18 due to an external pull up resistor.

6/ All input pins that are SERDES differential cannot be tested for IIL1_SH18 or IIH1_SH18 and LVPECL cannot be tested for IIL1_SP18 or IIH1_SP18 due to AC coupling capacitors on the test fixture.

7/ The Temperature Diode tests are performed for characterization purposes only.

8/ The INPUT_SSTL_25 pin group contains both the SSTL inputs and reference inputs. The IIL1_T25 and IIH1_T25 tests are not performed on the SSTL reference inputs. The SSTL reference inputs are only tested for IIH1_T25R.

9/ The following pins are not tested: CDRTGCNTOPIN[4:0] (G22, F19, F20, F21, F22), RXDDEBUGPIN[0] (G19), CDRTGCNTOCKPIN (G20), RXDDEBUGPIN[1] (H21) and RXDDEBUGPIN[0] (H22).

10/ SERDES VOD values will compute to ½ the expected value when tester resistance of 50ohms is included. The test program limits will be ½ limit value specified in the table.

11/ The SERDES VOS tests are performed for characterization purposes only.

12/ Input voltage levels are as follows, unless noted otherwise:

IN_CMOS_PN_18, IN_CMOS_PU_PN_18, IN_CMOS_PD_PN_18, IN_SCHM_PN_18,
BI_CMOS_PG_9MA_18: V_{IN} = 0.0V or VDD
IN_SERDES_LVPECL_18: V_{IN} = (VDD * 0.50) or VDD
IN_SERDES_DIFF_18: V_{IN} = (VDD * 0.50) or VDD
IN_SSTL_T_25: V_{IN} = (VDD2 * 0.5 – 0.6V) or (VDD2 * 0.5 + 0.6V)
IN_SSTL_REF_25: V_{IN} = 0.25V or VDD2 * 0.5

13/ Supply voltage levels are as follows, unless noted otherwise: VDD=1.71V and 1.89V; VDD2=2.3V and 2.7V

14/ ATPG masking:
Test all pins except: TD_ANODE, VREFRPIN, RXDDEBUGPIN[3], TXP0_A, TXP1_A, TXP2_A, TXP3_A, TXP0_B, TXP1_B, TXP2_B, TXP3_B, TXN0_A, TXN1_A, TXN2_A, TXN3_A, TXN0_B, TXN1_B, TXN2_B, TXN3_B

15/ BIST masking:
Test all pins except: TD_ANODE, VREFRPIN, MDIO, CMULOCKDETECTPIN

16/ FTHRU masking:
Test all pins except: TD_ANODE, VREFRPIN, LANESYNCSTATUSPIN, MDIO

17/ IDDQ_READS masking:
Test all pins except: TD_ANODE, VREFRPIN, RXALOSPIN

18/ TX_AMP masking:
Mask all pins except: TXP0_A, TXP1_A, TXP2_A, TXP3_A, TXP0_B, TXP1_B, TXP2_B, TXP3_B,TXN0_A, TXN1_A, TXN2_A, TXN3_A, TXN0_B, TXN1_B, TXN2_B, TXN3_B

19/ Test is performed per SERDES Lane, executed up to 50 times at each of six strobe times. Pass/Fail results are reported for first passing strobe and reported as the overall result for that lane test. If no passing execution is found at any of the 6 strobe points, the result is Fail.
String "_L0" in test name indicates SERDES Lane 0 tested,
String "_L1" in test name indicates SERDES Lane 1 tested,
String "_L2" in test name indicates SERDES Lane 2 tested,
String "_L3" in test name indicates SERDES Lane 3 tested,

20/ FTHRU Lane 0 only masking:
Test all pins except: TD_ANODE, VREFRPIN, MDIO, RXD1[9:0], RXD2[9:0], RXD3[9:0],COMDET1, COMDET2, COMDET3,RXERR1, RXERR2, RXERR3.
Note that the following pins are tested:RXD0[9:0], COMDET0, RXERR0, LANESYNCSTATUSPIN

21/ FTHRU Lane 1 only masking:
Test all pins except: TD_ANODE, VREFRPIN, MDIO, RXD0[9:0], RXD2[9:0], RXD3[9:0], COMDET0, COMDET2, COMDET3, RXERR0, RXERR2, RXERR3.
Note that the following pins are tested: RXD1[9:0], COMDET1, RXERR1, LANESYNCSTATUSPIN

22/ FTHRU Lane 2 only masking:
Test all pins except: TD_ANODE, VREFRPIN, MDIO, RXD0[9:0], RXD1[9:0], RXD3[9:0], COMDET0, COMDET1, COMDET3,RXERR0, RXERR1, RXERR3.
Note that the following pins are tested: RXD2[9:0], COMDET2, RXERR2, LANESYNCSTATUSPIN

23/ FTHRU Lane 3 only masking:
Test all pins except: TD_ANODE, VREFRPIN, MDIO, RXD0[9:0], RXD1[9:0],RXD2[9:0], COMDET0, COMDET1, COMDET2, RXERR0, RXERR1, RXERR2.
Note that the following pins are tested: RXD3[9:0], COMDET3, RXERR3, LANESYNCSTATUSPIN

24/ VDDA = -400mV during measurements only, otherwise VDDA = VDD during vector execution.

25/ The following entries have been tested as part of qualification. They are guaranteed by design but not tested on each part

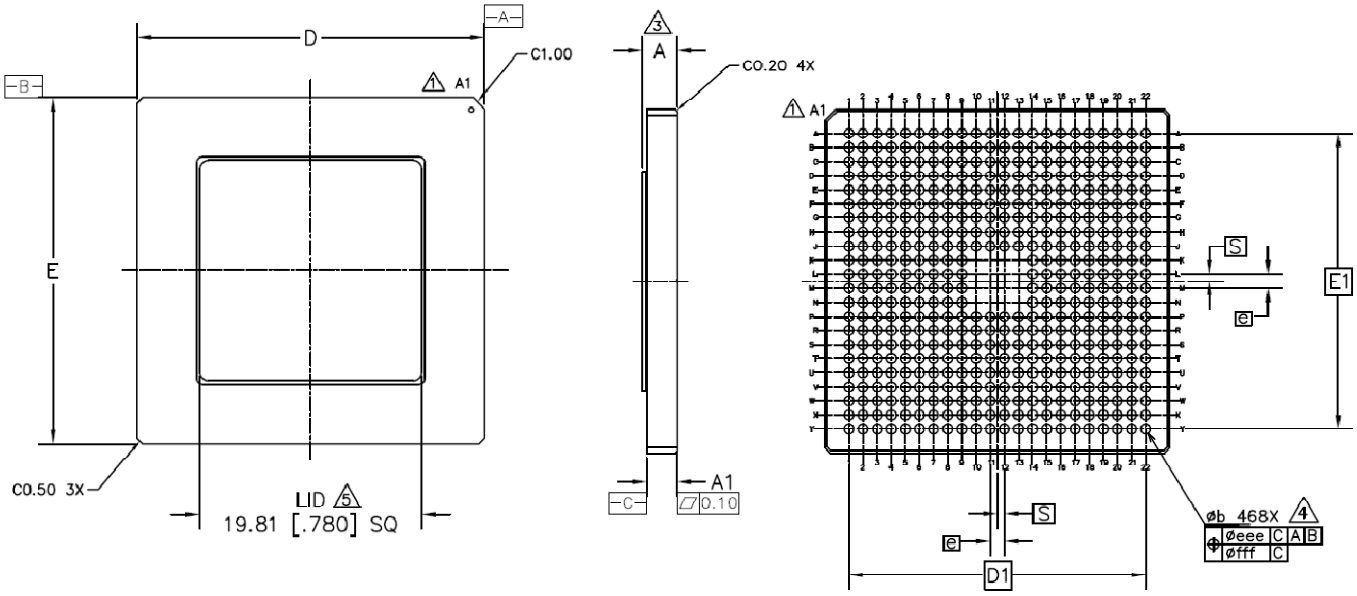
26/ Differential peak-to-peak. Pre-emphasis is disabled. Nominal

27/ Designed for an AC-coupled interface.

28/ Guaranteed by design; not tested on each part.

29/ Includes 0.10 UI of sinusoidal jitter

Case outline X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		3.43		.135	e	1.27 BSC		0.050 BSC	
A1	2.42	2.96	.095	.117	S	0.635 TYP		0.025 TYP	
b	0.81	0.91	.032	.036	eee	0.30 TYP		0.012 TYP	
D/E	30.80	31.20	1.213	1.228	fff	0.15 TYP		0.006 TYP	
D1/E1	26.67 TYP		1.050 TYP						

NOTES:

1. The A1 corner is identified by a larger chamfer and a dot on the top ceramic surface.
2. Controlling dimensions are in millimetres.
3. Distance from bottom of the ceramic to the top of the lid.
4. b = diameter of the metalized LGA pad.
5. LID CENTER ON PACKAGE.

FIGURE 1. Case outline.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
MDIO	B025	V4	B	BIDIRECTIONAL, CMOS, PROGRAMMABLE, 9MA, 1.8V	BI_CMOS_PG_9MA_18
MDCPIN	B028	T4	I	INPUT PIN, SCHMITT, PN, 1.8V	IN_SCHM_PN_18
REFCLK_N	R055	L6	I	INPUT PIN, SERDES LVPECL, 1.8V	IN_SERDES_LVPECL_18
REFCLK_P	R054	M6			
RXN0_A	R037	V1	I	INPUT PIN, SERDES, DIFFERENTIAL	IN_SERDES_DIFF_18
RXN0_B	R080	B2			
RXN1_A	R040	T1			
RXN1_B	R083	A3			
RXN2_A	R043	R2			
RXN2_B	R086	B5			
RXN3_A	R046	N1			
RXN3_B	R089	B7			
RXP0_A	R036	V2			
RXP0_B	R079	B1			
RXP1_A	R039	T2			
RXP1_B	R082	B3			
RXP2_A	R042	R1			
RXP2_B	R085	A5			
RXP3_A	R045	N2			
RXP3_B	R088	A7			
TCKPIN	L090	F4	I	INPUT, CMOS, PN, 1.8V	IN_CMOS_PN_18
TSTCLKPIN	L081	G6			
BGAPBYPASSPIN	L068	G17	I	INPUT, CMOS, PROGRAMMABLE, 1.8V, PD or PN	IN_CMOS_PD_PN_18
BITINVERTPIN	L054	N18			
BYPASSDECODEPIN	L050	P18			
BYPASSENCODEPIN	L049	P19			
BYPASSTXPCSPIN	L051	N22			
BYTEINVERTPIN	L055	N17			
CDRPRPIN[0]	L079	H5			
CDRPRPIN[1]	L078	H6			
CMUDIVPIN[0]	B013	T10			
DEBUGSELPIN[0]	L063	L17			
DEBUGSELPIN[2]	L061	M18			
DEBUGSELPIN[3]	L060	M19			
DVADDRPIN[0]	L088	F6			
DVADDRPIN[1]	L087	F7			
DVADDRPIN[2]	L086	G3	I	INPUT, CMOS, PROGRAMMABLE, 1.8V, PD or PN	IN_CMOS_PD_PN_18
DVADDRPIN[3]	L085	G4			
DVADDRPIN[4]	L082	G5			
ENPATTERNGEN0	L099	D4			
ENPATTERNGEN1	L098	D5			
ENPATTERNGEN2	L097	D6			

FIGURE 2. Terminal connections.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
ENPATTERNGEN3	L096	E4	I	INPUT, CMOS, PROGRAMMABLE, 1.8V, PD or PN	IN_CMOS_PD_PN_18
FIFORESETINPIN	L052	N21			
IDDQPIN	L067	H17			
LANESELPIN[0]	B037	R3			
LANESELPIN[1]	B034	R4			
LANESWAPPIN	L069	E22			
METENLOOPPIN	B038	P6			
MODEPIN[0]	B029	S6			
MODEPIN[2]	B031	S4			
PATTERNSELPIN[0]	B023	U5			
PATTERNSELPIN[1]	B022	V5			
PATTERNSELPIN[2]	B021	U6			
REFCLKSESELPIN	L058	M22			
REGFILERESETPIN	L053	N20			
RESETPIN	B032	S3			
RXALOSLVLPIN[1]	L072	A22			
RXEQONPIN	B040	P4			
RXEQPIN[2]	B043	N5			
RXRATESEL0PIN[0]	L032	T22			
RXRATESEL0PIN[1]	L031	T21			
RXRATESEL1PIN[0]	L036	S21			
RXRATESEL1PIN[1]	L035	S20			
RXRATESEL2PIN[0]	L042	R19			
RXRATESEL2PIN[1]	L041	R18			
RXRATESEL3PIN[0]	L046	P20			
RXRATESEL3PIN[1]	L045	P21			
SCANTSTPIN	L080	H3			
SERCDRENLOOPPIN	B039	P5			
TESTMODEPIN	L064	K17			
TXOASELPIN[2]	L016	T12			
TXPEPIN[0]	B016	T7			
TXPEPIN[1]	B015	T8			
TXPEPIN[2]	B014	T9			
TXRATESEL0PIN[0]	L028	T20			
TXRATESEL0PIN[1]	L027	T19			
TXRATESEL1PIN[0]	L034	S19			
TXRATESEL1PIN[1]	L033	S17			
TXRATESEL2PIN[0]	L040	R17			
TXRATESEL2PIN[1]	L037	S22			
TXRATESEL3PIN[0]	L044	R22			
TXRATESEL3PIN[1]	L043	R21			

FIGURE 2. Terminal connections - Continued.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
CDRPRPIN[2]	L077	J3	I	INPUT, CMOS, PROGRAMMABLE, 1.8V, PU or PN	IN_CMOS_PU_PN_18
CDRPRPIN[3]	L076	J4			
CMUDIVPIN[1]	L059	M20			
DEBUGSELPIN[1]	L062	M17			
MDIOSELPIN	B024	T5			
MODEPIN[1]	B030	S5			
PATTERNSELPIN[3]	B020	V6			
PORTSELPIN	B033	R6			
RXACCOUPLEDPIN	L015	T11			
RXALOSLVLPIN[0]	L073	J5			
RXEQPIN[0]	B041	P3			
RXEQPIN[1]	B042	N6			
TDIPIN	L091	F3			
TMSPIN	L089	F5			
TRSTBPIN	L095	E6			
TXOASELPIN[0]	L018	T14			
TXOASELPIN[1]	L017	T13			
TXCLK0	B105	Y10	I	INPUT, SSTL, 2.5V, TERMINATED LOAD	IN_SSTL_T_25
TXCLK1	B089	Y13			
TXCLK2	B071	Y17			
TXCLK3	B056	Y19			
TXD0[0]	B096	V11			
TXD0[1]	B098	X10			
TXD0[2]	B099	V10			
TXD0[3]	B101	Y9			
TXD0[4]	B102	X9			
TXD0[5]	B104	W9			
TXD0[6]	B107	V9			
TXD0[7]	B108	Y8			
TXD0[8]	B110	W8			
TXD0[9]	B111	V8			
TXD1[0]	B080	Y14			
TXD1[1]	B081	X14			
TXD1[2]	B083	W14	I	INPUT, SSTL, 2.5V, TERMINATED LOAD	IN_SSTL_T_25
TXD1[3]	B084	W13			
TXD1[4]	B086	V13			
TXD1[5]	B087	Y12			
TXD1[6]	B090	X12			
TXD1[7]	B092	W12			
TXD1[8]	B093	X11			
TXD1[9]	B095	W11			
TXD2[0]	B062	V18			
TXD2[1]	B064	X17			

FIGURE 2. Terminal connections - Continued.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
TXD2[2]	B065	W17	I	INPUT, SSTL, 2.5V, TERMINATED LOAD	IN_SSTL_T_25
TXD2[3]	B067	X16			
TXD2[4]	B068	W16			
TXD2[5]	B070	V16			
TXD2[6]	B073	Y15			
TXD2[7]	B074	X15			
TXD2[8]	B076	V15			
TXD2[9]	B077	V14			
TXD3[0]	B046	X21			
TXD3[1]	B047	W21			
TXD3[2]	B049	V20			
TXD3[3]	B050	X20			
TXD3[4]	B052	Y20			
TXD3[5]	B053	X19			
TXD3[6]	B055	W19			
TXD3[7]	B058	V19			
TXD3[8]	B059	Y18			
TXD3[9]	B061	W18			
TXN0_A	R021	Y7	O	OUTPUT PIN, SERDES, DIFFERENTIAL	OUTPUT_SERDES_DIFF_18
TXN0_B	R064	K2			
TXN1_A	R024	Y5			
TXN1_B	R067	H2			
TXN2_A	R027	X3			
TXN2_B	R070	F2			
TXN3_A	R030	X1			
TXN3_B	R073	D2			
TXP0_A	R020	X7			
TXP0_B	R063	K1			
TXP1_A	R023	X5			
TXP1_B	R066	H1			
TXP2_A	R026	Y3			
TXP2_B	R069	F1			
TXP3_A	R029	X2			
TXP3_B	R072	D1			
CMULOCKDETECTPIN	L023	V22	O	OUTPUT, CMOS, 3MA, 1.8V	OUTPUT_CMOS_3MA_18
CRASHDEBUGPIN	L026	T18			
DSALIGNSTATUSPIN	L022	Y22			
LANESYNCSTATUSPIN	L019	T15			
PCFRAMESYNCPIN	L025	T17			
PCMISMATCHPIN	L024	U22			
RXALOSPIN	B019	T6			

FIGURE 2. Terminal connections - Continued.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
CDRTGCNTOCKPIN	T020	G20	O	OUTPUT, SSTL, 2.5V, TERMINATED LOAD, LOW DRIVE	OUTPUT_LO_SSTL_T_25
CDRTGCNTOPIN[0]	T027	F22			
CDRTGCNTOPIN[1]	T026	F21			
CDRTGCNTOPIN[2]	T024	F20			
CDRTGCNTOPIN[3]	T023	F19			
CDRTGCNTOPIN[4]	T021	G22			
COMDET0	T030	A21			
COMDET1	T051	C18			
COMDET2	T073	A14			
COMDET3	T094	E11			
RXCLKN0	T038	A20			
RXCLKN1	T059	A16			
RXCLKN2	T081	B13			
RXCLKN3	T102	A9			
RXCLKP0	T039	B20			
RXCLKP1	T060	C16			
RXCLKP2	T082	C13			
RXCLKP3	T103	B9			
RXD0[0]	T048	D18			
RXD0[1]	T047	E18			
RXD0[2]	T045	E19			
RXD0[3]	T044	D19			
RXD0[4]	T042	B19			
RXD0[5]	T041	A19			
RXD0[6]	T036	C20			
RXD0[7]	T035	D20			
RXD0[8]	T033	E21			
RXD0[9]	T032	D21			
RXD1[0]	T069	D15			
RXD1[1]	T068	C15			
RXD1[2]	T066	B15			
RXD1[3]	T065	A15			
RXD1[4]	T063	E16			
RXD1[5]	T062	D16			
RXD1[6]	T057	E17			
RXD1[7]	T056	C17			
RXD1[8]	T054	B17			
RXD1[9]	T053	A17			
RXD2[0]	T091	C11			
RXD2[1]	T090	A11			
RXD2[2]	T088	E12			
RXD2[3]	T087	C12			

FIGURE 2. Terminal connections - Continued.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
RXD2[4]	T085	B12	O	OUTPUT, SSTL, 2.5V, TERMINATED LOAD, LOW DRIVE	OUTPUT_LO_SSTL_T_25
RXD2[5]	T084	A12			
RXD2[6]	T079	D13			
RXD2[7]	T078	E13			
RXD2[8]	T076	E14			
RXD2[9]	T075	D14			
RXD3[0]	T112	B8			
RXD3[1]	T111	C8			
RXD3[2]	T109	D8			
RXD3[3]	T108	E8			
RXD3[4]	T106	E9			
RXD3[5]	T105	D9			
RXD3[6]	T100	A10			
RXD3[7]	T099	B10			
RXD3[8]	T097	C10			
RXD3[9]	T096	D10			
RXDDEBUGPIN[0]	T018	G19			
RXDDEBUGPIN[1]	T017	H22			
RXDDEBUGPIN[2]	T015	H21			
RXDDEBUGPIN[3]	T014	H20			
RXDDEBUGPIN[4]	T012	J21			
RXDDEBUGPIN[5]	T011	J20			
RXDDEBUGPIN[6]	T009	J19			
RXDDEBUGPIN[7]	T008	K22			
RXDDEBUGPIN[8]	T006	K21			
RXDDEBUGPIN[9]	T005	K19			
RXERR0	T029	C21			
RXERR1	T050	B18			
RXERR2	T072	B14			
RXERR3	T093	D11			
VDD	-	A4	PWR	POWER, ANALOG	
	-	C4			
	-	Y4			
	-	W5			
	-	A6			
	-	C6			
	-	Y6			
	-	W7			
VDDA_R1_A	R032	K3	PWR	POWER, ANALOG	
VDDA_R1_B	R075	P1			
VDDA_R2_A	R034	E3			
VDDA_R2_B	R077	J1			
VDDA_R3_A	R048	A2			
VDDA_R3_B	R091	C1			
VDDA_RX1_A	R038	C3			
VDDA_RX1_B	R081	G1			
VDDA_RX2_A	R044	Y2			
VDDA_RX2_B	R087	E1			

FIGURE 2. Terminal connections - Continued.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
VDDA_T1_A	R019	W3	PWR	POWER, ANALOG	
VDDA_T1_B	R062	W1			
VDDA_TX1_A	R022	U3			
VDDA_TX1_B	R065	U1			
VDDA_TX2_A	R028	L3			
VDDA_TX2_B	R071	S1			
VDD	B002	N4	PWR	PWR	
	B004	K5			
	B006	D7			
	B008	H7			
	B010	K7			
	B012	M7			
	B018	P7			
	B027	S7			
	B036	G8			
	B045	J8			
	B114	L8			
	B116	N8			
	B118	R8			
	B120	H9			
	R001	S9			
	R004	G10			
	R006	R10			
	R008	H11			
	R010	S11			
	R011	G12			
	R013	R12			
	R015	H13			
	R017	S13			
	R093	G14			
	R095	R14			
	R097	H15			
	R099	K15			
	R101	M15			
	R103	P15			
	R105	S15			
	R107	G16			
	R109	J16			
	T120	L16			
	T118	N16			
	T116	R16			
	T114	T16			
	T002	P17			
	L108	R20			
	L106	M21			

FIGURE 2. Terminal connections - Continued.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
VDD	L104	-	PWR	PWR	
	L102	-			
	L100	-			
	L092	-			
	L083	-			
	L074	-			
	L065	-			
	L056	-			
	L047	-			
	L038	-			
	L029	-			
	L020	-			
	L013	-			
	L011	-			
	L009	-			
	L007	-			
	L005	-			
	L003	-			
	L002	-			
PLL_VDDA	R060	K6	PWR	PWR, ANALOG, PLL	
PLL_VDDD	R056	M5	PWR	PWR, DIGITAL, PLL	
VDD2	B051	A8	PWR	PWR, VDD2	
	B057	U8			
	B063	X8			
	B069	F9			
	B075	U9			
	B082	E10			
	B088	B11			
	B094	F11			
	B100	U11			
	B106	Y11			
	B112	V12			
	T110	F13			
	T104	U13			
	T098	C14			
	T092	F15			
	T086	U15			
	T080	W15			
	T074	D17			
	T070	F17			
	T064	U17			
	T058	A18			
	T052	G18			

FIGURE 2. Terminal connections - Continued.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
VDD2	T046	J18	PWR	PWR, VDD2	
	T040	L18			
	T034	X18			
	T028	H19			
	T022	U19			
	T016	E20			
	T010	L20			
	T004	B21			
VDD2	-	U21	PWR	PWR, VDD2	
	-	V21			
	-	Y21			
	-	J22			
	-	L22			
	-	X22			
ATB_N	R052	M4	X	ROUTETHROUGH, ANALOG, WITH IP	RTHRU_W_IP_18
ATB_P	R051	M3			
REXT	R057	L1			
RREF	R058	L4			
VBG_EXT	R050	M1			
VREFTPIN	B078	N3	I	SSTL, 2.5V, INPUT REFERENCE	IN_SSTL_REF_25
VREFRPIN	T071	J6	O	SSTL, 2.5V, OUTPUT REFERENCE	OUTPUT_SSTL_REF_25
ANODE_L071	L071	C22	O	TEMPERATURE DIODE, COLD SPARE, 1.8V	TDIODE_CS_18
CATHODE_L070	L070	D22	I		
TDOPIN	L094	E7	OZ	TRISTATE, CMOS, PROGRAMMABLE, 3MA, 1.8V	TRI_CMOS_RL_PN_3MA_18
VSS	B001	H4	GND	GND	
	B003	U4			
	B005	E5			
	B007	R5			
	B009	G7			
	B011	J7			
	B017	L7			
	B026	N7			
	B035	R7			
	B044	U7			
	B048	V7			
	B054	F8			
	B060	H8			
	B066	K8			
	B072	M8			
	B079	P8			
	B085	S8			

FIGURE 2. Terminal connections - Continued.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
VSS	B091	C9	GND	GND	
	B097	G9			
	B103	R9			
	B109	F10			
	B113	H10			
	B115	S10			
	B117	U10			
	B119	W10			
	R002	G11			
	R003	R11			
	R005	D12			
	R007	F12			
	R009	H12			
	R012	S12			
	R014	U12			
	R016	A13			
	R094	G13			
	R096	R13			
	R098	X13			
	R100	F14			
	R102	H14			
	R104	S14			
	R106	U14			
	R108	E15			
	T119	G15			
	T117	J15			
	T115	L15			
	T113	N15			
	T107	R15			
	T101	B16			
	T095	F16			
	T089	H16			
	T083	K16			
	T077	M16			
	T067	P16			
	T061	S16			
	T055	U16			
	T049	Y16			
	T043	J17			
	T037	V17			
	T031	F18			
	T025	H18			
	T019	K18			

FIGURE 2. Terminal connections - Continued.

Case outline X - Continued

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
VSS	T013	S18	GND	GND	
	T007	U18			
	T003	C19			
	T001	L19			
	L109	N19			
	L107	K20			
	L105	U20			
	L103	W20			
	L101	G21			
	L093	L21			
	L084	B22			
	L075	P22			
	L066	W22			
VSS	L057	-	GND	GND	
	L048	-			
	L039	-			
	L030	-			
	L021	-			
	L014	-			
	L012	-			
	L010	-			
	L008	-			
	L006	-			
	L004	-			
	L001	-			
VSS	-	J9	GND	GND	
	-	J10			
	-	J11			
	-	J12			
	-	J13			
	-	J14			
	-	K9			
	-	K14			
	-	L9			
	-	L14			
	-	M9			
	-	M14			
	-	N9			
	-	N14			
	-	P9			
	-	P10			
	-	P11			
	-	P12			

FIGURE 2. Terminal connections - Continued.

Signal name	PAD	PKG_PIN	SIG_type	Buffer_Description	Pin_Group
VSS	-	P13	GND	GND	
	-	P14			
VSSA	-	W4	GND	GND, ANALOG	
	-	X4			
	-	C5			
	-	B6			
	-	W6			
	-	X6			
	-	C7			
VSSA_1_A	R018	B4	GND	GND, ANALOG	
VSSA_1_B	R061	M2			
VSSA_2_A	R025	V3			
VSSA_2_B	R068	L2			
VSSA_3_A	R031	T3			
VSSA_3_B	R074	J2			
VSSA_4_A	R033	D3			
VSSA_4_B	R076	G2			
VSSA_5_A	R035	W2			
VSSA_5_B	R078	E2			
VSSA_6_A	R041	U2			
VSSA_6_B	R084	C2			
VSSA_7_A	R047	S2			
VSSA_7_B	R090	Y1			
VSSA_8_A	R049	P2			
VSSA_8_B	R092	A1			
PLL_VSSA	R059	K4	GND	GND, ANALOG, PLL	
PLL_VSSD	R053	L5	GND	GND, DIGITAL, PLL	

FIGURE 2. Terminal connections - Continued.

COLLECTION GROUP NAME	PREDEFINED GROUP NAMES
INPUT_CMOS_PN_18	IN_CMOS_PN_18, IN_SCHM_PN_18
INPUT_CMOS_PU_PN_18	IN_CMOS_PU_PN_18
INPUT_CMOS_PD_PN_18	IN_CMOS_PD_PN_18
TRI_BI_CMOS_PG_18	BI_CMOS_PG_9MA_18
TRI_BI_CMOS_RL_PN_18	TRI_CMOS_RL_PN_3MA_18
OUT_TRI_BI_CMOS_3MA_18	OUTPUT_CMOS_3MA_18, TRI_CMOS_RL_PN_3MA_18
OUT_TRI_BI_CMOS_9MA_18	BI_CMOS_PG_9MA_18
INPUT_BI_CMOS_18	IN_CMOS_PD_PN_18, IN_CMOS_PU_PN_18, IN_CMOS_PN_18, BI_CMOS_PG_9MA_18
INPUT_BI_SCHM_18	IN_SCHM_PN_18
INPUT_DIODE	TDIODE_CS_18
INPUT_SSTL_25	IN_SSTL_T_25, IN_SSTL_REF_25
INPUT_BI_SSTL_25	IN_SSTL_T_25
TRI_LO_BI_SSTL_25	OUTPUT_LO_SSTL_T_25
OUT_SSTL_REF_25	OUTPUT_SSTL_REF_25
INPUT_SERDES_LVPECL_18	IN_SERDES_LVPECL_18
INPUT_SERDES_DIFF_18	IN_SERDES_DIFF_18
OUT_SERDES_DIFF_18	OUTPUT_SERDES_DIFF_18
ROUTETHRU_W_IP_18	RTHRU_W_IP_18
IN&BI_CMOS_18	IN_CMOS_PD_PN_18, IN_CMOS_PU_PN_18, IN_CMOS_PN_18, IN_SCHM_PN_18, BI_CMOS_PG_9MA_18
OUT&BI_CMOS_18	OUTPUT_CMOS_3MA_18, BI_CMOS_PG_9MA_18

FIGURE 3. Pin Group Translation.

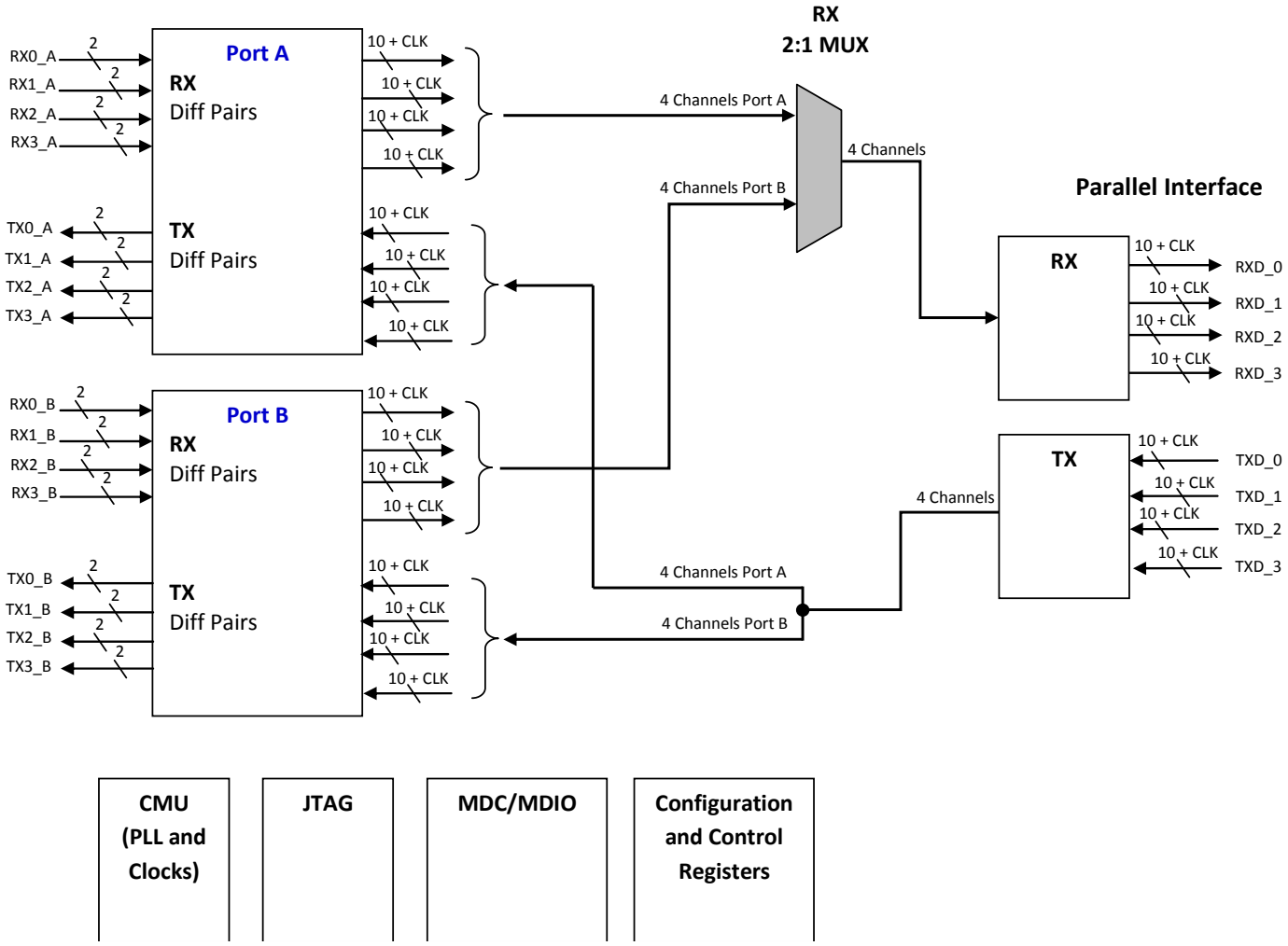
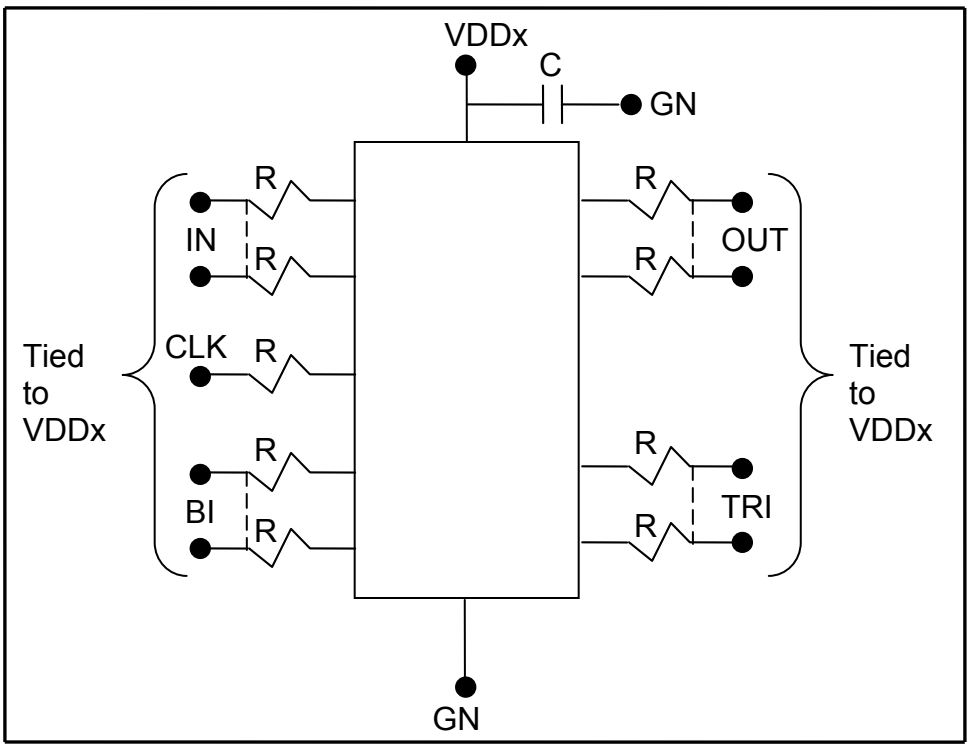


FIGURE 4. Block diagram.



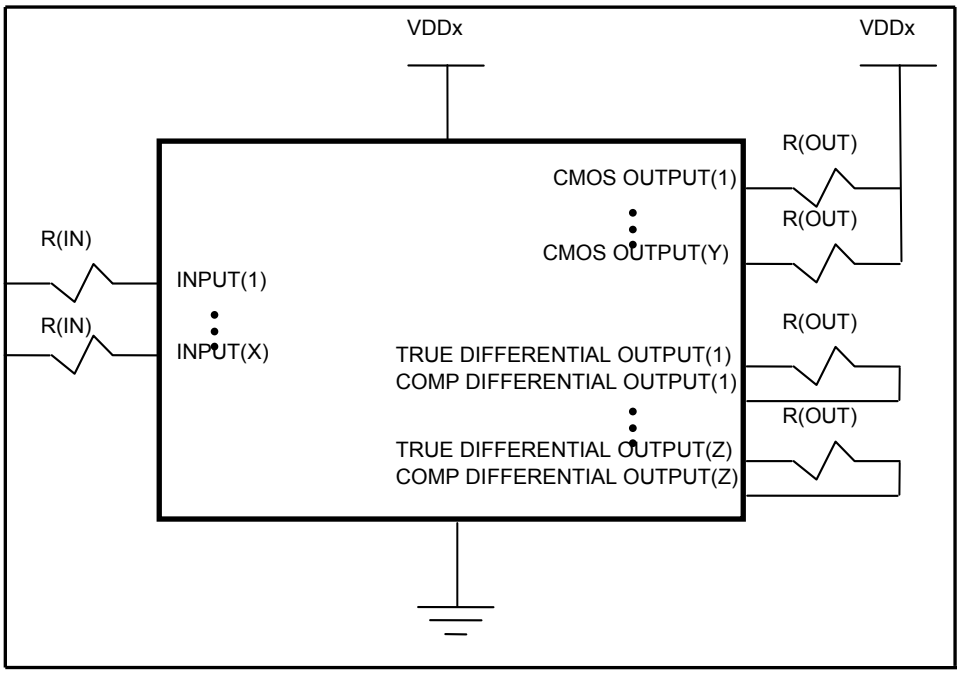
Notes

1. VDDx can be VDD, VDD2, and/or VDDA, as appropriate.
2. Device power pins (VDDx) connected to VDDx.
3. The absolute voltage ratings shall not be exceeded.
4. ESD precautions shall be followed.
5. Pin conditions

   VDDx = VDDMAX (VDD, VDD2, VDDA)
   VIH = VDD
   VIL = GND
   R = 2.2 Kohm (± 10 %)
   C = 0.1 µF (± 10%)
   IN = Inputs
   OUT = Outputs
   TRI = Tri-State Outputs
   BI = Bidirectionals (Input/Output)
   CLK = System Clock

   Note: Individual pins may need to be configured differently (e.g. for LVDS inputs VIL = GND) and would follow the static burn-in setup conditions.

FIGURE 5. Radiation exposure circuit.



General

- VDDx can be VDD, VDD2, and/or VDDA, as appropriate. Power supply tolerances are ± 0.1 V.
- R(IN) = depends on the I/O buffer type (ranges from 75 Ω to 1 KΩ , ± 5%, 0.25W)
- R(OUT) = depends on the I/O buffer type (ranges from 75 Ω to 1 KΩ, ± 5%, 0.25W)
- No device pin will share a resistor with any other device pin.
- The burn-in board will have sufficient VDDx to GND bypass capacitance besides above circuit.
- Static Burn-in will use same hardware as Dynamic Burn-in.

Static Burn-in

- All pins are pulled as follows through individual series resistors during the entire static burn-in test:
  - CMOS pins are pulled to levels of VDDx or VSS.
  - LVPECL pins are pulled as follows: Complement pin held at 1.16 V, and True pin low is 0.78 V and True pin high is 1.52 V. Voltage divider resistor tolerances and wattages are ± 5%, 0.25W, respectively.
- Device is in the power-up logic state during static burn-in if it contains no memories. If the device contains memories they are put into the true state for one half of the static burn-in, and in the complement state for the second half of the static burn-in.

Dynamic Burn-in

- All pins are pulled in the same fashion as static burn-in during the entire dynamic burn-in. If the pin is connected to a burn-in driver it may also undergo toggling.

FIGURE 6. Burn-in circuit.

Trivor DC INPUTS Vector Table

	Vector Set				Vector Set	
Pin	VIL	VIH		Pin	VIL	VIH
CMUDIVPIN[0]	ATPG_0	ATPG_0		RXP0_A	TX_AMP_100NS	TX_AMP_100NS
TXPEPIN[2]	ATPG_0	ATPG_0		RXN0_A	TX_AMP_100NS	TX_AMP_100NS
TXPEPIN[1]	ATPG_0	ATPG_0		RXP1_A	TX_AMP_100NS	TX_AMP_100NS
TXPEPIN[0]	ATPG_0	ATPG_0		RXN1_A	TX_AMP_100NS	TX_AMP_100NS
PATTERNSELPIN[3]	ATPG_0	ATPG_0		RXP2_A	TX_AMP_100NS	TX_AMP_100NS
PATTERNSELPIN[2]	ATPG_0	ATPG_0		RXN2_A	TX_AMP_100NS	TX_AMP_100NS
PATTERNSELPIN[1]	ATPG_0	ATPG_0		RXP3_A	TX_AMP_100NS	TX_AMP_100NS
PATTERNSELPIN[0]	ATPG_0	ATPG_0		RXN3_A	TX_AMP_100NS	TX_AMP_100NS
MDIOSELPIN	Not sensitized	ATPG_0		REFCLK_P	FT_1GE_A	FT_1GE_A
MDCPIN	Not sensitized	Not sensitized		REFCLK_N	FT_1GE_A	FT_1GE_A
MODEPIN[0]	ATPG_0	ATPG_0		RXP0_B	TX_AMP_100NS	TX_AMP_100NS
MODEPIN[1]	ATPG_0	ATPG_0		RXN0_B	TX_AMP_100NS	TX_AMP_100NS
MODEPIN[2]	ATPG_0	ATPG_0		RXP1_B	TX_AMP_100NS	TX_AMP_100NS
RESETPIN	ATPG_0	ATPG_0		RXN1_B	TX_AMP_100NS	TX_AMP_100NS
PORTSELPIN	Not sensitized	ATPG_0		RXP2_B	TX_AMP_100NS	TX_AMP_100NS
LANESELPIN[1]	ATPG_0	ATPG_0		RXN2_B	TX_AMP_100NS	TX_AMP_100NS
LANESELPIN[0]	ATPG_0	ATPG_0		RXP3_B	TX_AMP_100NS	TX_AMP_100NS
METENLOOPPIN	Not sensitized	Not sensitized		RXN3_B	TX_AMP_100NS	TX_AMP_100NS
SERCDRENLOOPPIN	Not sensitized	Not sensitized		ENPATTERNGEN0	ATPG_0	ATPG_0
RXEQONPIN	Not sensitized	Not sensitized		ENPATTERNGEN1	ATPG_0	ATPG_0
RXEQPIN[0]	ATPG_0	ATPG_0		ENPATTERNGEN2	ATPG_0	ATPG_0
RXEQPIN[1]	ATPG_0	ATPG_0		ENPATTERNGEN3	ATPG_0	ATPG_0
RXEQPIN[2]	ATPG_0	ATPG_0		TRSTBPIN	Not sensitized	Not sensitized
TXD3[0]	FT_1GE_A	FT_1GE_A		TDIPIN	Not sensitized	Not sensitized
TXD3[1]	FT_1GE_A	FT_1GE_A		TCKPIN	Not sensitized	Not sensitized
TXD3[2]	FT_1GE_A	FT_1GE_A		TMSPIN	Not sensitized	Not sensitized
TXD3[3]	FT_1GE_A	FT_1GE_A		DVADDRPIN[0]	Not sensitized	Not sensitized
TXD3[4]	FT_1GE_A	FT_1GE_A		DVADDRPIN[1]	Not sensitized	Not sensitized
TXD3[5]	FT_1GE_A	FT_1GE_A		DVADDRPIN[2]	Not sensitized	Not sensitized
TXD3[6]	FT_1GE_A	FT_1GE_A		DVADDRPIN[3]	Not sensitized	Not sensitized
TXCLK3	FT_1GE_A	FT_1GE_A		DVADDRPIN[4]	Not sensitized	Not sensitized
TXD3[7]	FT_1GE_A	FT_1GE_A		TSTCLKPIN	ATPG_0	ATPG_0
TXD3[8]	FT_1GE_A	FT_1GE_A		SCANTSTPIN	Not sensitized	Not sensitized
TXD3[9]	FT_1GE_A	FT_1GE_A		CDRPRPIN[0]	Not sensitized	Not sensitized
TXD2[0]	FT_1GE_A	FT_1GE_A		CDRPRPIN[1]	Not sensitized	Not sensitized

FIGURE 7. Functional Test Vectors

Trivor DC INPUTS Vector Table - Continued

	Vector Set	
Pin	VIL	VIH
TXD2[1]	FT_1GE_A	FT_1GE_A
TXD2[2]	FT_1GE_A	FT_1GE_A
TXD2[3]	FT_1GE_A	FT_1GE_A
TXD2[4]	FT_1GE_A	FT_1GE_A
TXD2[5]	FT_1GE_A	FT_1GE_A
TXCLK2	FT_1GE_A	FT_1GE_A
TXD2[6]	FT_1GE_A	FT_1GE_A
TXD2[7]	FT_1GE_A	FT_1GE_A
TXD2[8]	FT_1GE_A	FT_1GE_A
TXD2[9]	FT_1GE_A	FT_1GE_A
VREFTPIN	Not sensitized	Not sensitized
TXD1[0]	FT_1GE_A	FT_1GE_A
TXD1[1]	FT_1GE_A	FT_1GE_A
TXD1[2]	FT_1GE_A	FT_1GE_A
TXD1[3]	FT_1GE_A	FT_1GE_A
TXD1[4]	FT_1GE_A	FT_1GE_A
TXD1[5]	FT_1GE_A	FT_1GE_A
TXCLK1	FT_1GE_A	FT_1GE_A
TXD1[6]	FT_1GE_A	FT_1GE_A
TXD1[7]	FT_1GE_A	FT_1GE_A
TXD1[8]	FT_1GE_A	FT_1GE_A
TXD1[9]	FT_1GE_A	FT_1GE_A
TXD0[0]	FT_1GE_A	FT_1GE_A
TXD0[1]	FT_1GE_A	FT_1GE_A
TXD0[2]	FT_1GE_A	FT_1GE_A
TXD0[3]	FT_1GE_A	FT_1GE_A
TXD0[4]	FT_1GE_A	FT_1GE_A
TXD0[5]	FT_1GE_A	FT_1GE_A
TXCLK0	FT_1GE_A	FT_1GE_A
TXD0[6]	FT_1GE_A	FT_1GE_A
TXD0[7]	FT_1GE_A	FT_1GE_A
TXD0[8]	FT_1GE_A	FT_1GE_A
TXD0[9]	FT_1GE_A	FT_1GE_A
TXOASELPIN[0]	Not sensitized	Not sensitized
TXOASELPIN[1]	Not sensitized	Not sensitized
TXOASELPIN[2]	Not sensitized	Not sensitized
LANESWAPPIN	Not sensitized	Not sensitized
RXACCOUPLEDPIN	Not sensitized	Not sensitized

	Vector Set	
Pin	VIL	VIH
CDRPRPIN[2]	Not sensitized	Not sensitized
CDRPRPIN[3]	Not sensitized	Not sensitized
RXALOSLVLPIN[0]	Not sensitized	Not sensitized
RXALOSLVLPIN[1]	Not sensitized	Not sensitized
BGAPBYPASSPIN	Not sensitized	Not sensitized
IDDQPIN	ATPG_0	Not sensitized
TESTMODEPIN	Not sensitized	ATPG_0
DEBUGSELPIN[0]	ATPG_0	ATPG_0
DEBUGSELPIN[1]	ATPG_0	ATPG_0
DEBUGSELPIN[2]	ATPG_0	ATPG_0
DEBUGSELPIN[3]	ATPG_0	ATPG_0
CMUDIVPIN[1]	ATPG_0	ATPG_0
REFCLKSESELPIN	Not sensitized	Not sensitized
BYTEINVERTPIN	ATPG_0	ATPG_0
BITINVERTPIN	ATPG_0	ATPG_0
REGFILERESETPIN	ATPG_0	ATPG_0
FIFORESETINPIN	ATPG_0	ATPG_0
BYPASSTXPCSPIN	ATPG_0	ATPG_0
BYPASSDECODEPIN	ATPG_0	ATPG_0
BYPASSENCODEPIN	ATPG_0	ATPG_0
RXRATESEL3PIN[0]	ATPG_0	ATPG_0
RXRATESEL3PIN[1]	ATPG_0	ATPG_0
TXRATESEL3PIN[0]	ATPG_0	ATPG_0
TXRATESEL3PIN[1]	ATPG_0	ATPG_0
RXRATESEL2PIN[0]	ATPG_0	ATPG_0
RXRATESEL2PIN[1]	ATPG_0	ATPG_0
TXRATESEL2PIN[0]	ATPG_0	ATPG_0
TXRATESEL2PIN[1]	ATPG_0	ATPG_0
RXRATESEL1PIN[0]	ATPG_0	ATPG_0
RXRATESEL1PIN[1]	ATPG_0	ATPG_0
TXRATESEL1PIN[0]	ATPG_0	ATPG_0
TXRATESEL1PIN[1]	ATPG_0	ATPG_0
RXRATESEL0PIN[0]	ATPG_0	ATPG_0
RXRATESEL0PIN[1]	ATPG_0	ATPG_0
TXRATESEL0PIN[0]	ATPG_0	ATPG_0
TXRATESEL0PIN[1]	ATPG_0	ATPG_0
TD_CATHODE	Not sensitized	Not sensitized

FIGURE 7. Functional Test Vectors – Continued.

Trivor DC OUTPUTS Vector Table

		Vector Set				Vector Set	
Pin	IO Type	VOL	VOH	Pin	IO Type	VOL	VOH
MDIO	Bipad	IDDQ_READS	IDDQ_READS	RXD2[5]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXALOSPIN	CMOS_OUT	ATPG_PATT_0	ATPG_PATT_0	RXCLKP2	SSTL_O	ATPG_0	ATPG_0
TXP0_A	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXCLKN2	SSTL_O	ATPG_0	ATPG_0
TXN0_A	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD2[6]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXP1_A	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD2[7]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXN1_A	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD2[8]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXP2_A	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD2[9]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXN2_A	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	COMDET2	SSTL_O	ATPG_0	ATPG_0
TXP3_A	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXERR2	SSTL_O	ATPG_0	ATPG_0
TXN3_A	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD1[0]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXP0_B	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD1[1]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXN0_B	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD1[2]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXP1_B	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD1[3]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXN1_B	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD1[4]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXP2_B	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD1[5]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
TXN2_B	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXCLKP1	SSTL_O	ATPG_0	ATPG_0
TXP3_B	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXCLKN1	SSTL_O	ATPG_0	ATPG_0
TXN3_B	HS_SERIAL	TX_AMP_100NS	TX_AMP_100NS	RXD1[6]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD3[0]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD1[7]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD3[1]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD1[8]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD3[2]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD1[9]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD3[3]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	COMDET1	SSTL_O	ATPG_0	ATPG_0
RXD3[4]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXERR1	SSTL_O	ATPG_0	ATPG_0
RXD3[5]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD0[0]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXCLKP3	SSTL_O	ATPG_0	ATPG_0	RXD0[1]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXCLKN3	SSTL_O	ATPG_0	ATPG_0	RXD0[2]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD3[6]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD0[3]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD3[7]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD0[4]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD3[8]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD0[5]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD3[9]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXCLKP0	SSTL_O	ATPG_0	ATPG_0
COMDET3	SSTL_O	ATPG_0	ATPG_0	RXCLKN0	SSTL_O	ATPG_0	ATPG_0
RXERR3	SSTL_O	ATPG_0	ATPG_0	RXD0[6]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD2[0]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD0[7]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD2[1]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD0[8]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD2[2]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXD0[9]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH
RXD2[3]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	COMDET0	SSTL_O	ATPG_0	ATPG_0
RXD2[4]	SSTL_O	FT_1GFC_LOW	FT_1GFC_HIGH	RXERR0	SSTL_O	ATPG_0	ATPG_0

FIGURE 7. Functional Test Vectors – Continued.

Trivor DC OUTPUTS Vector Table - Continued

		Vector Set	
Pin	IO Type	VOL	VOH
CDRTGCNTOPIN[0]	SSTL_O	Not Conditioned	Not Conditioned
CDRTGCNTOPIN[1]	SSTL_O	Not Conditioned	Not Conditioned
CDRTGCNTOPIN[2]	SSTL_O	Not Conditioned	Not Conditioned
CDRTGCNTOPIN[3]	SSTL_O	Not Conditioned	Not Conditioned
CDRTGCNTOPIN[4]	SSTL_O	Not Conditioned	Not Conditioned
CDRTGCNTOCKPIN	SSTL_O	Not Conditioned	Not Conditioned
RXDDEBUGPIN[0]	SSTL_O	Not Conditioned	Not Conditioned
RXDDEBUGPIN[1]	SSTL_O	Not Conditioned	Not Conditioned
RXDDEBUGPIN[2]	SSTL_O	Not Conditioned	Not Conditioned
RXDDEBUGPIN[3]	SSTL_O	ATPG_PATT_0	ATPG_PATT_0
RXDDEBUGPIN[4]	SSTL_O	ATPG_PATT_0	ATPG_PATT_0
RXDDEBUGPIN[5]	SSTL_O	ATPG_PATT_0	ATPG_PATT_0
RXDDEBUGPIN[6]	SSTL_O	ATPG_PATT_0	ATPG_PATT_0
RXDDEBUGPIN[7]	SSTL_O	ATPG_PATT_0	ATPG_PATT_0
RXDDEBUGPIN[8]	SSTL_O	ATPG_PATT_0	ATPG_PATT_0
RXDDEBUGPIN[9]	SSTL_O	ATPG_PATT_0	ATPG_PATT_0
CRASHDEBUGPIN	CMOS_OUT	ATPG_PATT_0	ATPG_PATT_0
PCFRAMESYNCPIN	CMOS_OUT	ATPG_PATT_0	ATPG_PATT_0
PCMISMATCHPIN	CMOS_OUT	ATPG_PATT_0	ATPG_PATT_0
CMULOCKDETECTPIN	CMOS_OUT	ATPG_PATT_0	ATPG_PATT_0
DSALIGNSTATUSPIN	CMOS_OUT	ATPG_PATT_0	ATPG_PATT_0
LANESYNCSTATUSPIN	CMOS_OUT	ATPG_PATT_0	ATPG_PATT_0

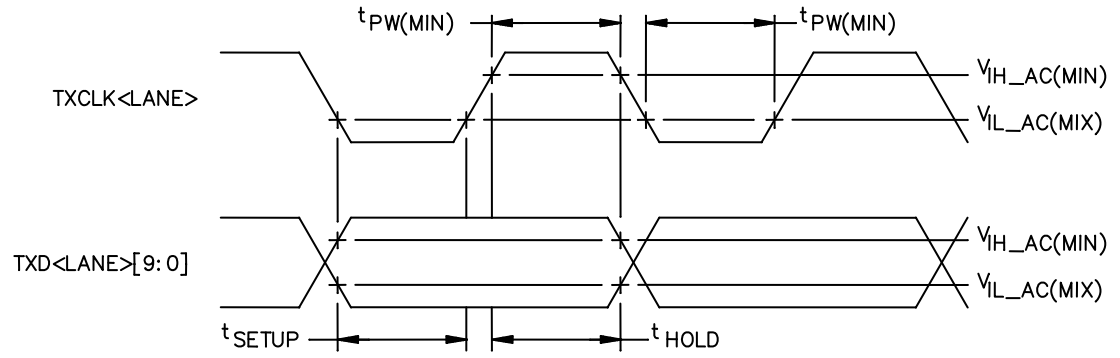
FIGURE 7. Functional Test Vectors – Continued.

Trivor Functional Vectors

Functional Vectors	Conditions 3/, 13/	Tester Period (ns)	Frequency (MHz)	Type
ATPG_PATT_0, ATPG_0, ATPG_1, ATPG_2, ATPG_3, ATPG_4, ATPG_5, ATPG_6, ATPG_7, ATPG_8, ATPG_9	See Note 14/	100.00	10.0	Pass/Fail
BIST_D10_FR_9P4	See Note 15/	9.41	106.4	Pass/Fail
BIST_D10_FR_6P4	See Note 15/	6.4	156.3	Pass/Fail
BIST_D10_FR_8P0	See Note 15/	8.0	125.0	Pass/Fail
BIST_D10_HR_9P4	See Note 15/	9.40	106.3	Pass/Fail
BIST_D10_HR_8P0	See Note 15/	8.0	125.0	Pass/Fail
BIST_D15_FR_9P4	See Note 15/	9.41	106.4	Pass/Fail
BIST_D10_FR_6P2	See Note 15/	6.2	161.3	Char Info Only
BIST_D10_HR11P5	See Note 15/	11.5	87.0	Char Info Only
BIST_D10_QR_8P0	See Note 15/	8.0	125.0	Char Info Only
BIST_D15_FR17P2	See Note 15/	17.2	58.1	Char Info Only
BIST_D15_FR_9P2	See Note 15/	9.2	108.7	Char Info Only
BIST_D20_FR12P5	See Note 15/	12.5	80.0	Char Info Only
BIST_D20_FR16P0	See Note 15/	16.0	62.5	Char Info Only
FTHRU_1GFC_HIGH	See Note 16/	8.00	125.0	Pass/Fail
FTHRU_1GFC_LOW	See Note 16/	8.00	125.0	Pass/Fail
IDDQ_READS	See Note 17/	10.00	100.0	Pass/Fail
ATPG_IDDQ_C3	See Note 14/	100.00	10.0	Pass/Fail
TX_AMP_10NS_ST1	See Note 18/	5.00	200.0	Pass/Fail
TX_AMP_10NS_ST2	See Note 18/	5.00	200.0	Pass/Fail
TX_AMP_100NS	See Note 18/	50.00	20.0	Pass/Fail
FT_1GEA_L0_S	See Note 19/ 20/	-0.5	6.5	StrobeMul
FT_1GEA_L0_T	See Note 19/ 20/	-0.5	50	Trials
FT_1GEA_L1_S	See Note 19/ 21/	-0.5	6.5	StrobeMul
FT_1GEA_L1_T	See Note 19/ 21/	-0.5	50	Trials
FT_1GEA_L2_S	See Note 19/ 22/	-0.5	6.5	StrobeMul
FT_1GEA_L2_T	See Note 19/ 22/	-0.5	50	Trials
FT_1GEA_L3_S	See Note 19/ 23/	-0.5	6.5	StrobeMul
FT_1GEA_L3_T	See Note 19/ 23/	-0.5	50	Trials
FT_1GEB_L0_S	See Note 19/ 20/	-0.5	6.5	StrobeMul
FT_1GEB_L0_T	See Note 19/ 20/	-0.5	50	Trials
FT_1GEB_L1_S	See Note 19/ 21/	-0.5	6.5	StrobeMul
FT_1GEB_L1_T	See Note 19/ 21/	-0.5	50	Trials
FT_1GEB_L2_S	See Note 19/ 22/	-0.5	6.5	StrobeMul
FT_1GEB_L2_T	See Note 19/ 22/	-0.5	50	Trials
FT_1GEB_L3_S	See Note 19/ 23/	-0.5	6.5	StrobeMul
FT_1GEB_L3_T	See Note 19/ 23/	-0.5	6.5	Trials

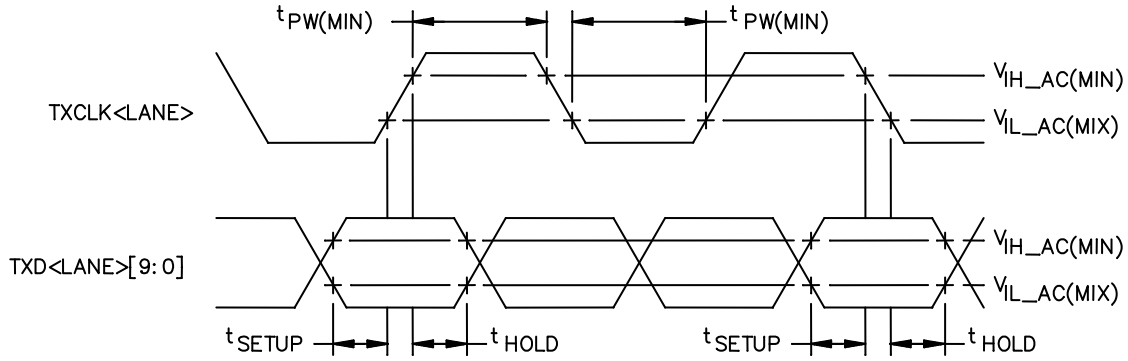
Note references in Figure 7 are located at the end of Table 1 – Electrical Performance Characteristics.

FIGURE 7. Functional Test Vectors – Continued.



TRANSMIT SDR TIMING DIAGRAM FOR PARALLEL INTERFACE

FIGURE 8. SSTL-2 AC timing waveforms.



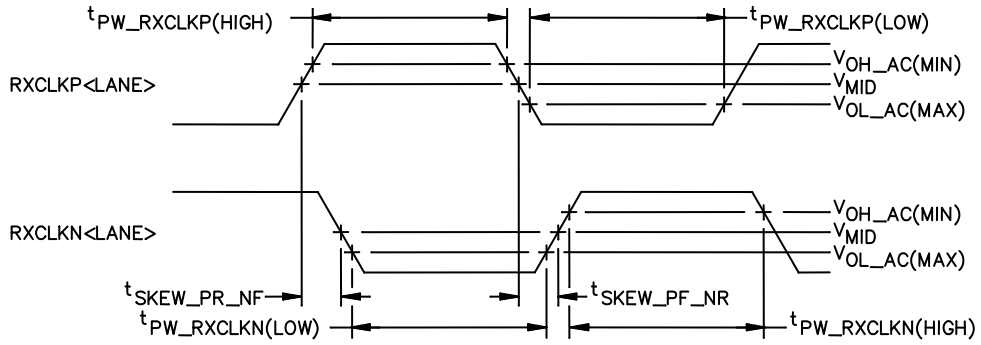
TRANSMIT DDR TIMING DIAGRAM FOR PARALLEL INTERFACE

Transit timing parameters

Symbol	TXCLK/TXD	Units
t_{setup}	-810	ps
t_{hold}	1620	ps
t_{pwmin}	2.5	ns

NOTE:
1. The TXCLK and TXD relationship are for the SSTL receive buffers on the parallel receive side. The “RX” nomenclature is in re;lation to the serial interface.

FIGURE 9. SSTL-2 AC timing waveforms.



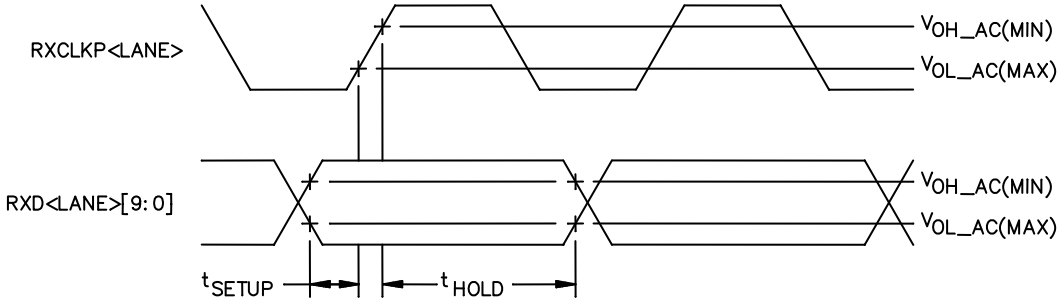
RXCLKP TO RXCLKN TIMING DIAGRAM

Receive clock timing parameters

Symbol	Lane0	Lane1	Lane2	Lane3	Units
$t_{pw\_rxclkp(high)}$ Min	3070	2910	2880	3330	ps
$t_{pw\_rxclkp(low)}$ Min	3130	3160	3170	2880	ps
$t_{pw\_rxclkn(low)}$ Min	3150	2990	2960	3340	ps
$t_{pw\_rxclkn(high)}$ Min	3070	3110	3130	2860	ps
$t_{skew\_pr\_nf}$ Max	130	130	150	180	ps
$t_{skew\_pf\_nr}$ Max	210	200	230	200	ps

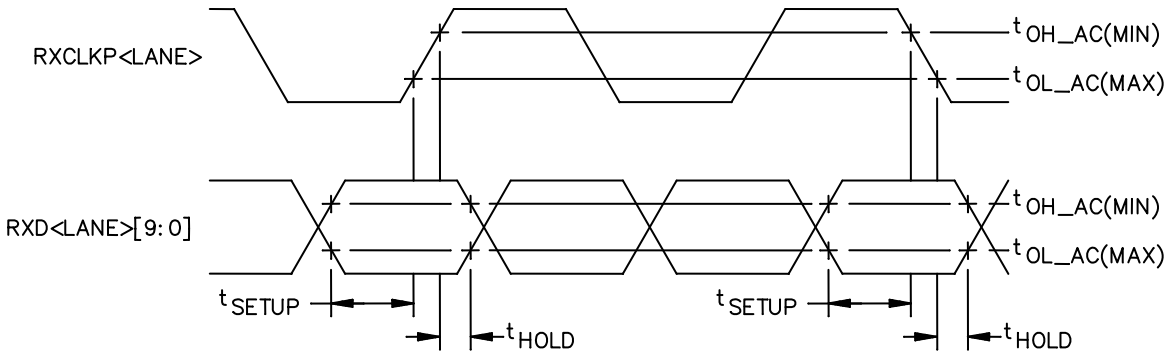
NOTES:
1. The pulse widths shown are measured with the fastest supported speed or Trivor representing a worst case.
2. Pulse width increase as speed decreases.

FIGURE 10. SSTL-2 AC timing waveforms.



RECEIVED SDR TIMING DIAGRAM FOR PARALLEL INTERFACE

FIGURE 11. SSTL-2 AC timing waveforms.



RECEIVE DDR TIMING DIAGRAM FOR PARALLEL INTERFACE

Receive timing parameters

	Symbol	Lane0	Lane1	Lane2	Lane3	Units
SDR	T_{setup}	4660	4480	4300	4800	ps
	T_{hold}	390	320	730	330	ps
DDR	T_{setup}	1590	1570	1420	1470	ps
	T_{hold}	390	320	730	330	ps

NOTES:
1. T The hold times shown are measured with the fastest supported speed or Trivor representing a worst case.
2. Hold time will increase as speed decreases, setup times will remain constant.
3. The setup and hold times shown are between RXCLKP and the receive data.
3. SDR hold time is the DDR hold time increased by the minimum pulse width high of the RXCLK

FIGURE 12. SSTL-2 AC timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, method 5012 (see 1.5 herein).

TABLE IIA. Electrical test requirements.

Line number	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Pre burn-in	1, 2, 3, 4, 5, 6, 7, 8A,8B	1, 2, 3, 4, 5, 6, 7, 8A,8B	1, 2, 3, 4, 5, 6, 7, 8A, 8B
2	Interim electrical parameters			1, 7
4	Final electrical parameters (see 4.2)	1*, 2, 3, 4, 5, 6, 7*, 8A, 8B Δ	1*, 2, 3, 4, 5, 6, 7*, 8A, 8B Δ	1*, 2, 3, 4, 5, 6, 7*, 8A, 8B Δ
5	Group A test requirements (see 4.4)	1*, 2, 3, 4, 5, 6, 7*, 8A, 8B Δ	1*, 2, 3, 4, 5, 6, 7*, 8A, 8B Δ	1*, 2, 3, 4, 5, 6, 7*, 8A, 8B Δ
6	Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8A, 8B	1, 2, 3, 4, 5, 6, 7, 8A, 8B	1, 2, 3, 4, 5, 6, 7, 8A, 8B
7	Group D end-point electrical parameters (see 4.4)	1,4,7	1,4,7	1,4,7
8	Group E end-point electrical parameters (see 4.4)	1,4,7	1,4,7	1,4,7

Notes

1/ Any or all subgroups may be combined when using high-speed testers.

2/ Subgroups 7 and 8 functional tests shall verify the truth table.

3/ * indicates PDA applies to subgroup 1 and 7.

4/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

TABLE IIB. Delta characteristics.

Test (1)	Condition	Symbol	Delta Limit	Units
VDD2 Quiescent Supply Current	T_A =-55^{O}C	ΔIDD_Q_25	±100	µA
VDD Quiescent Supply Current	T_A =-55^{O}C	ΔIDD_Q_18	±100	µA
VDDA Quiescent Supply Current	T_A =25^{O}C	ΔIDD_Q_18A	±100	µA

Notes:

(1) Delta is applied from each successive insertion into burn-in.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D or E . The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition B and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 1 x10^4 and 5 x 10^6 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C. The latchup test temperature shall be at an elevated operating temperature of 100°C to 125°C.

f. Bias conditions shall be V_{DD} = 3.0 V dc for the upset measurements and V_{DD} = 3.6 V dc for the latchup measurements.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0547.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-09-01

Approved sources of supply for SMD 5962-10208 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H1020801VXC	34168	HXSRD01TVH
5962H1020801QXC	34168	HXSRD01TQH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell 12001 State Highway 55 Plymouth, MN 55441