REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made changes to Table IA, parameters: I_{DDDOP3}, I_{DDDOP1}, $I_{DDDOPW1}$, $I_{DDOPW40}$, $I_{DDDOPW40}$, I_{DDOPR1}, $I_{DDDOPR1}$, $I_{DDOPR40}$, $I_{DDDOPR40}$, C_{INA}, C_{INC}. ksr	08-12-12	Robert M. Heber
B	Made changes to Table IA, parameters: Standby current CS disabled (I_{DDSB2}), from 25mA to 30 mA, and Standby current enabled (I_{DDSB}) from 25 mA to 30 mA. ksr	09-07-17	Charles Saffle
C	Added device type 02 a 1.5 V capable device. Updated boilerplate to current MIL-PRF-38535 requirements and removed all class M references. Correct Figure 4 test circuit and max junction temperature TJ from 150ºC to 175ºC in 1.3. Made editorial changes to sections 1.2.2, 1.4, 1.6, Table 1A and Table 1B, Table IIB. lht	13-06-12	Charles Saffle
D	Changed V_{DD}/V_{DDD} Voltage Ramp Time in 1.4. Corrected Table IA test conditions for $I_{DDDOPR1}$ and $I_{DDDOPR40}$. Added footnotes to clarify figure 1. Corrected Figures 4 and 5. Corrected footnote sequence in table IB. Updated drawing to current MIL-PRF-38535 requirements. - lhl	14-03-12	Charles Saffle
E	Corrections to Tables IIA and IIB, update to current requirements. – llb	18-07-27	Charles Saffle

REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E	E	E	E									
SHEET	15	16	17	18	19	20	21	22	23	24	25									

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Cheri Rida

APPROVED BY
Robert M. Heber

DRAWING APPROVAL DATE
08-07-08

REVISION LEVEL
E

MICROCIRCUIT, MEMORY, DIGITAL, CMOS/SOI, 2M x 8-BIT, RADIATION-HARDENED, LOW VOLTAGE SRAM, MONOLITHIC SILICON

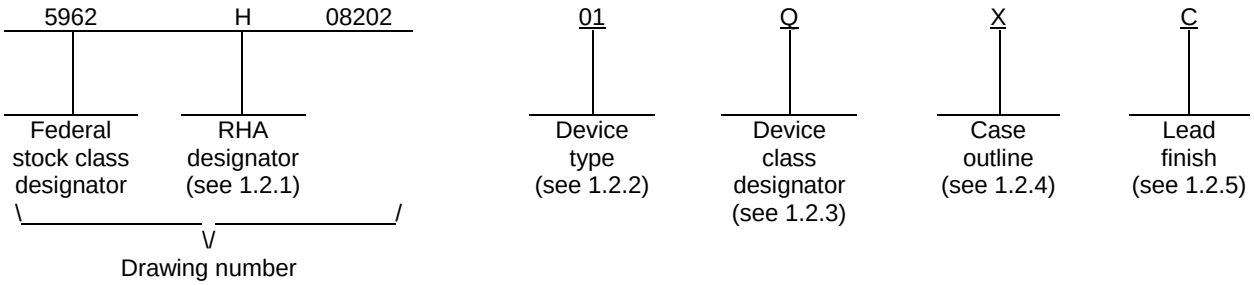
SIZE	CAGE CODE	
A	**67268**	**5962-08202**

SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01 1/	HXSR01608-A(Q or V)H	2M X 8-bit rad-hard CMOS/SOI SRAM	20 ns
02 1/	HLXSR01608-A(Q or V)H	2M X 8-bit rad-hard CMOS/SOI SRAM	25 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	40	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ See Table IA for conditions that clarify access times.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range I/O (V_{DDD}) .....-0.5 V dc to +4.4 V dc
Supply voltage range Core (V_{DD}) .....-0.5 V dc to +2.4 V dc
DC input voltage range (V_{IN}) .....-0.5 V dc to V_{DDD} + 0.5 V dc
DC output voltage range (V_{OUT}) .....-0.5 V dc to V_{DDD} + 0.5 V dc
DC or average output current (I_{OUT}).....15 mA
Storage temperature .....-65°C to +150°C
Lead temperature (soldering 5 seconds) .....+270°C
Thermal resistance, junction to case (Θ_{JC}) .....2.0 °C/W
Output voltage applied to high Z-state .....-0.5 V dc to V_{DDD} + 0.5V dc
Maximum power dissipation .....2.5 W
Case operating temperature range (T_C) .....-55ºC to +125ºC
Maximum junction temperature (T_J) 175ºC

1.4 Recommended operating conditions. 4/

Supply voltage range I/O (V_{DDD}) .....3.0 V dc to 3.6 V dc
Optional Supply voltage range I/O (V_{DDD})(Device type 01) .....2.3 V dc to 2.7 V dc
Supply voltage range Core (V_{DD}) .....1.65 V dc to 1.95 V dc
Optional Supply voltage range Core (V_{DD})(Device type 02).....1.35 V dc to 1.65 V dc
Supply voltage reference (V_{SS}) .....0.0 V dc
High level input voltage range (V_{IH}) .....0.7 x V_{DDD} to V_{DDD} + 0.3 V dc
Low level input voltage range (V_{IL}) .....-0.3 V dc to 0.3 x V_{DDD}
Voltage on any pin (V_{IN}) .....-0.3 V dc to V_{DDD} + 0.3
Power Down Time .....5 ms minimum
Power Up Ramp Time (V_{DDD} & V_{DD}) .....1 x 10^{-5} to 1.0 second
Case operating temperature range (T_C) .....-55ºC to +125ºC

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, method 5012)…….. 100 percent

1.6 Radiation features. 5/.

For device types 01 and 02:
Maximum total dose available (dose rate = 50-300 rad (Si/s)……..1 Mrads (Si)

Single event phenomenon (SEP) (see 4.4.4.4):
Heavy ion No SEL at an effective LET…….≤ 120 MeV-cm2/mg
Heavy Ion Single event upset (SEU) rate .....1 x 10^{-12} upsets/bit-day 6/
Proton Single event upset (SEU) rate for device type 01 ……..2 x 10^{-12} upsets/bit-day 6/
Proton Single event upset (SEU) rate for device type 02 ……..5 x 10^{-12} upsets/bit-day 6/
Neutron irradiation .....1 x 10^{14} neutrons/cm2 7/
Dose rate induced upset.....1 x 10^{10} rad(Si)/sec for < 50 nsec
Dose rate survivability.....1 x 10^{12} rad(Si)/sec for < 50 nsec
Latch-up.....Immune by SOI technology

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ All voltages are referenced to V_{SS}.

4/ Maximum applied voltage shall not exceed 4.4 V.

5/ For details RHA parameters and test results, contact the device manufacturer.

6/ Projected performance based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield using Weibull parameters derived from actual test data (see 4.4.4.4). Weibull parameters are available from the vendor to calculate projected upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).

7/ Guaranteed but not tested for 1MeV equivalent neutrons.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on Figure 3.

3.2.4 Output load circuit. The output load circuit for functional tests shall be as specified on Figure 4.

3.2.5 Tester timing characteristics and timing waveforms. The tester AC timing characteristics and timing waveforms shall be as specified on Figure 5 and applies to capacitance, read cycle, and write cycle measurements unless otherwise specified.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ or $2.3\ V \le V_{DDD} \le 3.7\ V$ and $1.65\ V \le V_{DD} \le 1.95\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Device type 01							
Standby Current – NCS disabled	I_{DDSB2} I_{DDDSB2}	f=0MHz, NCS, NOE, NWE = V_{DDD}	1, 2, 3	01		30.0 0.3	mA
Standby Current –enabled	I_{DDSB} I_{DDDSB}	f=0MHz, NCS, NOE, NWE=V_{SS}	1, 2, 3	01		30.0 0.3	mA
Operating Supply Current Disabled, address bus at max frequency 3/	I_{DDOP3} I_{DDDOP3}	f=40MHz, NCS, NOE, NWE = V_{DDD}	1, 2, 3	01		2 5	mA
Operating Supply Current Deselected, write mode 3/	I_{DDOP1} I_{DDDOP1}	NCS, NOE = V_{DDD}, 1MHz NWE vector controlled	1, 2, 3	01		0.1 0.2	mA
Operating Supply Current Selected, write mode low frequency 3/	I_{DDOPW1} $I_{DDDOPW1}$	f=1MHz, NCS=V_{SS}, NOE=V_{DDD}, NWE vector controlled	1, 2, 3	01		2 0.2	mA
Operating Supply Current Selected, write mode high frequency 3/	$I_{DDOPW40}$ $I_{DDDOPW40}$	f=40MHz, NCS=V_{SS}, NOE=V_{DDD}, NWE vector controlled	1, 2, 3	01		80 8.0	mA
Operating Supply Current Selected, read mode low frequency 3/	I_{DDOPR1} $I_{DDDOPR1}$	f=1MHz, NCS=V_{SS}, NOE, NWE =V_{DDD}	1, 2, 3	01		1.0 0.2	mA
Operating Supply Current Selected, read mode high frequency 3/	$I_{DDOPR40}$ $I_{DDDOPR40}$	f=40MHz, NCS=V_{SS}, NOE, NWE =V_{DDD}	1, 2, 3	01		40 8.0	mA
Data Retention Current	I_{DR1} I_{DR2}	V_{DD} = 1.0 V V_{DDD} = 2.0 V	1, 2, 3	01		20 0.2	mA
Low level output voltage	V_{OL}	V_{DDD} = 3.0 V, V_{DD} = 1.65 V, I_{OL}=10mA, V_{IL} =V_{SS}, V_{IH} = V_{DDD}	1, 2, 3	01		0.4	V
High level output voltage	V_{OH}	V_{DDD} = 3.0 V, V_{DD} =1.65 V, I_{OH}=-5mA, V_{IL} = V_{SS}, V_{IH} = V_{DDD}	1, 2, 3	01	2.7		V
Input leakage current	I_{ILK}	V_{IN} = 3.6 V, V_{DDD} = 3.6 V, V_{DD} = 1.95 V, all other pins at 3.6 V	1, 2, 3	01		5	µA
Output leakage current	I_{OLK}	V_{OUT} = 3.6V, V_{DDD} = 3.6 V, V_{DD} = 1.95 all other pins at 3.6 V	1, 2, 3	01		10	µA
Input capacitance (address and control) 4/	C_{INA} C_{INC} C_{NCS}	V_{IN} = V_{DDD} or V_{SS}, f = 1 MHz See 4.4.1e	4	01		7 17 20	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ or $2.3\ V \le V_{DDD} \le 3.7\ V$ and $1.65\ V \le V_{DD} \le 1.95\ V$ $V_{IH}=V_{DDD}$, $V_{IL}=V_{SS}$ unless otherwise specified See figures 4 and 5	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Device type 01							
Output capacitance 4/	C_{OUT}		4	01		7	pF
Functional tests		See 3.2.7 and 4.4.1.c	7, 8	01			
Data retention voltage	V_{DR}	V_{DDD} = 2.0 V, V_{DD} = 1.0 V	7, 8	01	5/		
Read cycle time	t_{AVAVR}	$3.0\ V \le V_{DDD} \le 3.6\ V$, $1.65\ V \le V_{DD} \le 1.95\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$, $1.65\ V \le V_{DD} \le 1.95\ V$	9, 10, 11	01	20 22		ns
Address access time	t_{AVQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$, $1.65\ V \le V_{DD} \le 1.95\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$, $1.65\ V \le V_{DD} \le 1.95\ V$	9, 10, 11	01		20 22	ns
Address change output invalid time	t_{AXQX}		9, 10, 11	01	4		ns
Chip select access time	t_{SLQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$, $1.65\ V \le V_{DD} \le 1.95\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$, $1.65\ V \le V_{DD} \le 1.95\ V$	9, 10, 11	01		20 22	ns
Chip select to output enable time	t_{SLQX}		9, 10, 11	01	0		ns
Chip select to output disable time	t_{SHQZ}		9, 10, 11	01		4	ns
Output enable access time	t_{GLQV}		9, 10, 11	01		6	ns
Output enable to output active time	t_{GLQX}		9, 10, 11	01	0		ns
Output enable to output disable time	t_{GHQZ}		9, 10, 11	01		4	ns
Write cycle time	t_{AVAVW}		9, 10, 11	01	12		ns
Minimum write enable pulse width	t_{WLWH}		9, 10, 11	01	7		ns
Chip select to end of write time	t_{SLWH}		9, 10, 11	01	10		ns
Data valid to end of write time	t_{DVWH}		9, 10, 11	01	6		ns
Address valid to end of write time	t_{AVWH}		9, 10, 11	01	12		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ or $2.3\ V \le V_{DDD} \le 2.7\ V$ and $1.65\ V \le V_{DD} \le 1.95\ V$ $V_{IH}=V_{DDD}$, $V_{IL}=V_{SS}$ unless otherwise specified See figures 4 and 5	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Device type 01							
Data hold time after end of write time	t_{WHDX}		9, 10, 11	01	0		ns
Address valid setup to start of write time	t_{AVWL}		9, 10, 11	01	0		ns
Address valid hold after end of write time	t_{WHAX}		9, 10, 11	01	0		ns
Write enable to output disable time	t_{WLQZ}		9, 10, 11	01		4	ns
Write disable to output enable time	t_{WHQX}		9, 10, 11	01	0		ns
Write disable write enable pulse width 6/	t_{WHWL}		9, 10, 11	01	5		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ and $1.35\ V \le V_{DD} \le 1.65\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Device type 02							
Standby Current – NCS disabled	I_{DDSB2} I_{DDDSB2}	f=0MHz, NCS, NOE, NWE = V_{DDD}	1, 2, 3	02		30.0 0.3	mA
Standby Current –enabled	I_{DDSB} I_{DDDSB}	f=0MHz, NCS, NOE, NWE=V_{SS}	1, 2, 3	02		30.0 0.3	mA
Operating Supply Current Disabled, address bus at max frequency 3/	I_{DDOP3} I_{DDDOP3}	f=40MHz, NCS, NOE, NWE = V_{DDD}	1, 2, 3	02		2 5	mA
Operating Supply Current Deselected, write mode 3/	I_{DDOP1} I_{DDDOP1}	NCS, NOE = V_{DDD}, 1MHz NWE vector controlled	1, 2, 3	02		0.1 0.15	mA
Operating Supply Current Selected, write mode low frequency 3/	I_{DDOPW1} $I_{DDDOPW1}$	f=1MHz, NCS=V_{SS}, NOE=V_{DDD}, NWE vector controlled	1, 2, 3	02		2 0.2	mA
Operating Supply Current Selected, write mode high frequency 3/	$I_{DDOPW40}$ $I_{DDDOPW40}$	f=40MHz, NCS=V_{SS}, NOE=V_{DDD}, NWE vector controlled	1, 2, 3	02		68 8.0	mA
Operating Supply Current Selected, read mode low frequency 3/	I_{DDOPR1} $I_{DDDOPR1}$	f=1MHz, NCS=V_{SS}, NOE, NWE =V_{DDD}	1, 2, 3	02		1.0 0.2	mA
Operating Supply Current Selected, read mode high frequency 3/	$I_{DDOPR40}$ $I_{DDDOPR40}$	f=40MHz, NCS=V_{SS}, NOE, NWE =V_{DDD}	1, 2, 3	02		34 8.0	mA
Data Retention Current	I_{DR1} I_{DR2}	V_{DD} = 1.0 V V_{DDD} = 2.0 V	1, 2, 3	02		20 0.2	mA
Low level output voltage	V_{OL}	V_{DDD} = 3.0 V, V_{DD} = 1.35 V, I_{OL}=10mA, V_{IL} =V_{SS}, V_{IH} = V_{DDD}	1, 2, 3	02		0.4	V
High level output voltage	V_{OH}	V_{DDD} = 3.0 V, V_{DD} =1.35 V, I_{OH}=-5mA, V_{IL} = V_{SS}, V_{IH} = V_{DDD}	1, 2, 3	02	2.7		V
Input leakage current	I_{ILK}	V_{IN} = 3.6 V, V_{DDD} = 3.6 V, V_{DD} = 1.95 V, all other pins at 3.6 V	1, 2, 3	02		5	µA
Output leakage current	I_{OLK}	V_{OUT} = 3.6V, V_{DDD} = 3.6 V, V_{DD} = 1.95 all other pins at 3.6 V	1, 2, 3	02		10	µA
Input capacitance (address and control) 4/	C_{INA} C_{INC} C_{NCS}	V_{IN} = V_{DDD} or V_{SS}, f = 1 MHz See 4.4.1e	4	02		7 17 20	pF
Output capacitance 4/	C_{OUT}		4	02		7	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ and $1.35\ V \le V_{DD} \le 1.65\ V$ $V_{IH}=V_{DDD}$, $V_{IL}=V_{SS}$ unless otherwise specified See figures 4 and 5	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Device type 02							
Functional tests		See 3.2.7 and 4.4.1.c	7, 8	02			
Data retention voltage	V_{DR}	V_{DDD} = 2.0 V, V_{DD} = 1.0 V	7, 8	02	5/		
Read cycle time	t_{AVAVR}		9, 10, 11	02	25		ns
Address access time	t_{AVQV}		9, 10, 11	02		25	ns
Address change output invalid time	t_{AXQX}		9, 10, 11	02	4		ns
Chip select access time	t_{SLQV}		9, 10, 11	02		25	ns
Chip select to output enable time	t_{SLQX}		9, 10, 11	02	0		ns
Chip select to output disable time	t_{SHQZ}		9, 10, 11	02		4	ns
Output enable access time	t_{GLQV}		9, 10, 11	02		6	ns
Output enable to output active time	t_{GLQX}		9, 10, 11	02	0		ns
Output enable to output disable time	t_{GHQZ}		9, 10, 11	02		4	ns
Write cycle time	t_{AVAVW}		9, 10, 11	02	12		ns
Minimum write enable pulse width	t_{WLWH}		9, 10, 11	02	7		ns
Chip select to end of write time	t_{SLWH}		9, 10, 11	02	12		ns
Data valid to end of write time	t_{DVWH}		9, 10, 11	02	6		ns
Address valid to end of write time	t_{AVWH}		9, 10, 11	02	12		ns
Data hold time after end of write time	t_{WHDX}		9, 10, 11	02	0		ns
Address valid setup to start of write time	t_{AVWL}		9, 10, 11	02	0		ns
Address valid hold after end of write time	t_{WHAX}		9, 10, 11	02	0		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ and $1.35\ V \le V_{DD} \le 1.65\ V$ $V_{IH}=V_{DDD}$, $V_{IL}=V_{SS}$ unless otherwise specified See figures 4 and 5	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Device type 02							
Write enable to output disable time	t_{WLQZ}		9, 10, 11	02		4	ns
Write disable to output enable time	t_{WHQX}		9, 10, 11	02	0		ns
Write disable write enable pulse width 6/	t_{WHWL}		9, 10, 11	02	5		ns

1/ Pre-irradiation values for RHA marked devices shall also be the post-irradiation values unless otherwise specified.
2/ When performing post-irradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$.
3/ These dynamic operating mode current measurements (I_{DDOPx} and I_{DDDOPx}) exclude standby mode currents (I_{DDS} and I_{DDDS}).
4/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ As verified by functional tests.
6/ Guaranteed but not tested.

TABLE IB. SEP Test Limits 1/ 2/ 3/

Device Type	ION Type	Memory pattern	Bias V_{DD} = 1.65 V Device 01 Bias V_{DD} = 1.35 V Device 02 SEU Rate Adam's 90% environment 4/	Bias V_{DD} =1.95 V Device 01 Bias V_{DD}=1.65 V Device 02 No latch-up (SEL) Effective LET
01, 02	Heavy ion	5/	1 x 10^{-12} upsets/bit-day 6/	LET ≤ 120 MeV/mg/cm^2
01	Proton	5/	2 x 10^{-12} upsets/bit-day 7/	-
02	Proton	5/	5 x 10^{-12} upsets/bit-day 7/	-

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ For SEL worst case temperature T_A = +125°C± 10°C and for SEU worst case temperature T_A = +25°C±10°C.
4/ Based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield. Weibull parameters available from the vendor to calculate upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).
5/ Testing shall be performed using checkerboard and checkerboard bar test patterns.
6/ Weibull parameters are available from the vendor upon request.
7/ The proton test is performed at the energy level 200 MeV and CRÈME 96 with Weibull parameters. Weibull parameters are available from the vendor upon request.

Case outline X

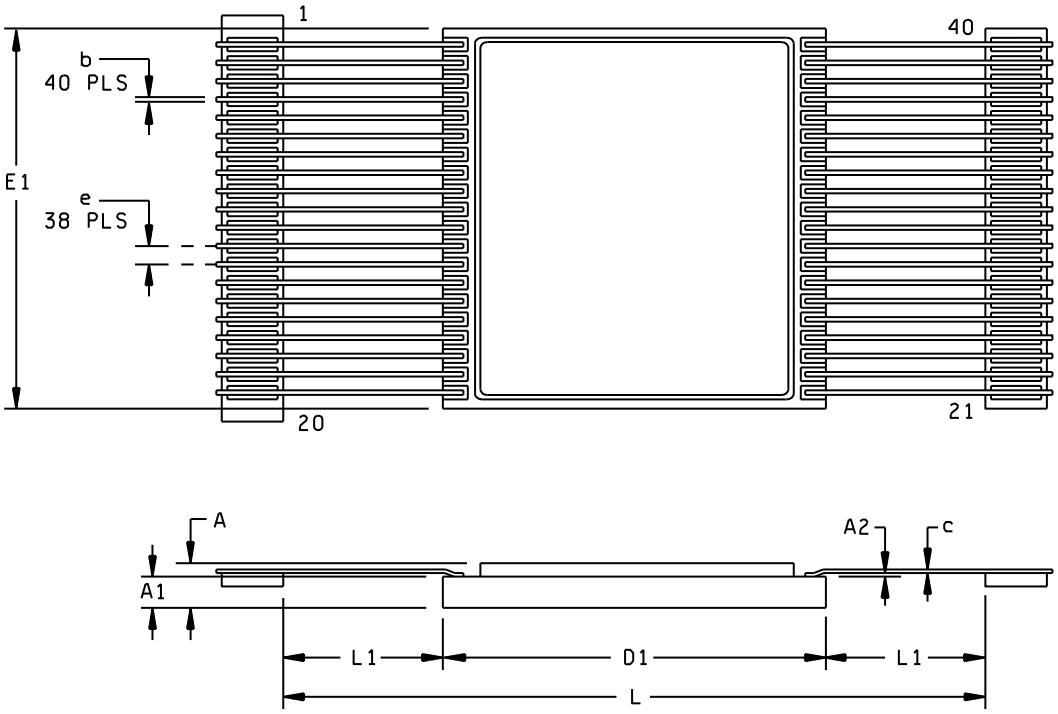


FIGURE 1. Case outline.

Symbol	Millimeters			Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.62	2.87	3.13	.102	.112	.122
A1	2.17	2.41	2.65	.086	.095	.104
b	0.41	0.46	0.51	.016	.018	.020
c	0.10	0.15	0.20	.004	.006	.008
D1	21.47	21.67	21.87	.845	.853	.891
e	1.14	1.27	1.40	.045	.050	.055
E1	25.45	25.65	25.82	1.002	1.010	1.018
L	---	40.89	---	---	1.610	---
L1	9.25	9.61	---	.364	.379	---
L2	3.10	3.30	3.50	.122	.130	.138

1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. All exposed metalized areas are gold plated over electroplated nickel.
3. Package lid is electrically connected to V_{SS} for package X.
4. The package is assembled with four on package CDR33 chip capacitors 0.1uF with 50V rating which meet approved criteria and are similar to MIL-PRF-123 capacitors. Two capacitors placed between V_{DD} and V_{SS} and two between V_{DDD} and V_{SS} to improve noise sensitivity for I/O switching and dose rate hardness. A2 is height of package including the capacitors.
5. Tie bar measurements are for reference only.

FIGURE 1. Case outline - Continued.

Device types	All
Case outlines	X
Terminal number	Terminal symbol
1	V_{SS}
2	A0
3	A1
4	A2
5	A3
6	A4
7	NCS
8	D0
9	D1
10	V_{DDD}
11	V_{SS}
12	D2
13	D3
14	NWE
15	A5
16	A6
17	A7
18	A8
19	A9
20	V_{DD}
21	V_{SS}
22	A10
23	A11
24	A12
25	A13
26	A14
27	A15
28	D4
29	D5
30	V_{DDD}
31	V_{SS}
32	D6
33	D7
34	NOE
35	A16
36	A17
37	A18
38	A19
39	A20
40	V_{DD}

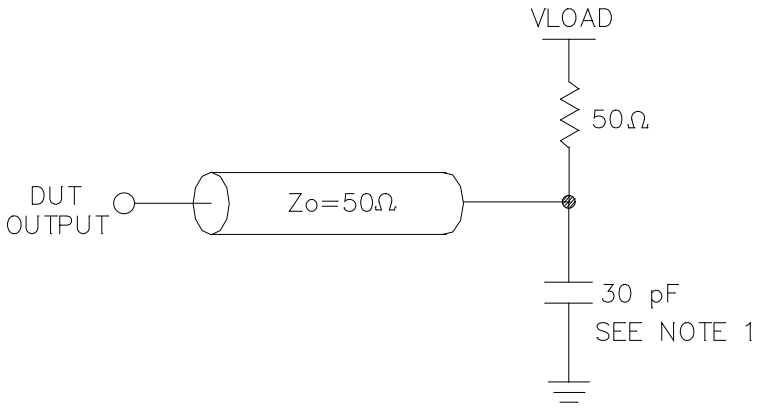
FIGURE 2. Terminal connections.

NCS	NWE	NOE	MODE	DQ
L	H	L	READ	Data Out
L	L	X	WRITE	Data In
H	X	X	Deselected	High Z

Note: L=low, H=high, X=low or high

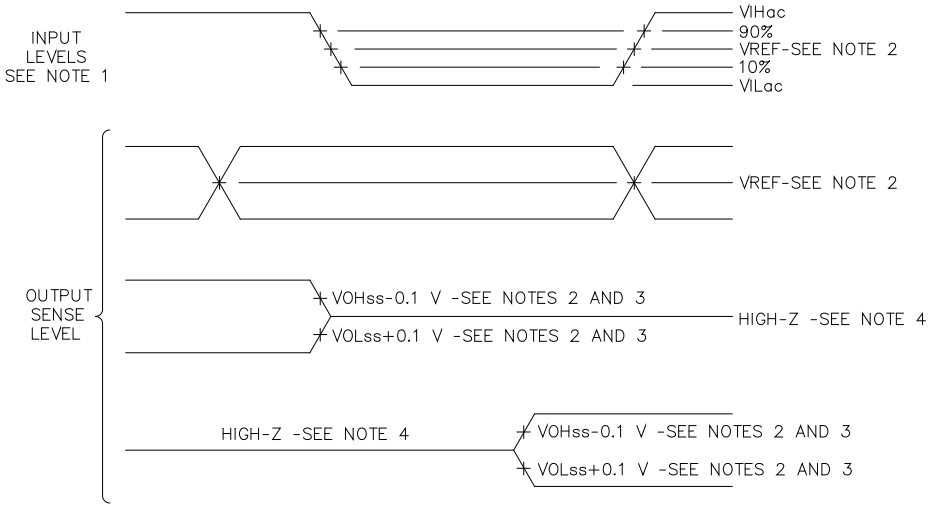
FIGURE 3. Truth table.

AC Timing Output Load Circuit



NOTE 1: Set to 5 pF for T*QZ (Low-Z to High-Z) timing parameters.

I/O	VLOAD
3.3 V	$V_{DDD}/2$
2.5 V	$V_{DDD}/2$



1. All input rise and fall times = 1 ns between the 90% and 10% levels
2. Timing parameter reference voltage level.
3. ss: Low-Z V_{OH} and V_{OL} steady state output voltage.
4. High-Z Output pin pulled to V_{LOAD} by output load circuit.

I/O type	$V_{IH}ac$	$V_{IL}ac$	V_{REF}	V_{LOAD}
3.3 V CMOS	V_{DDIO}	V_{SS}	$V_{DDIO}/2$	$V_{DDIO}/2$
2.5 V CMOS	V_{DDIO}	V_{SS}	$V_{DDIO}/2$	$V_{DDIO}/2$

FIGURE 4. Output load circuit

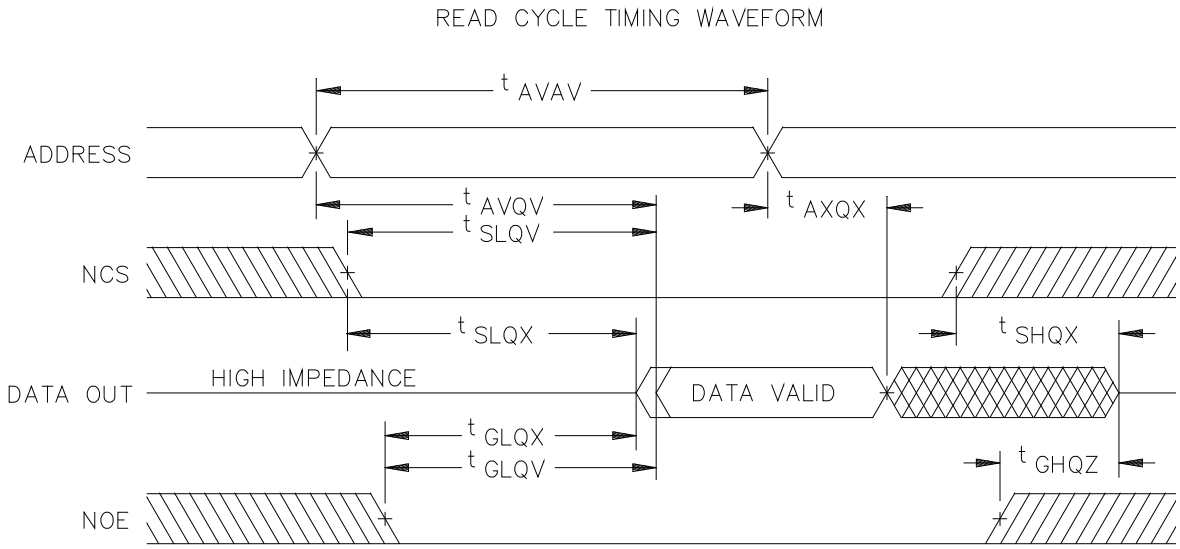


FIGURE 5. Timing waveforms.

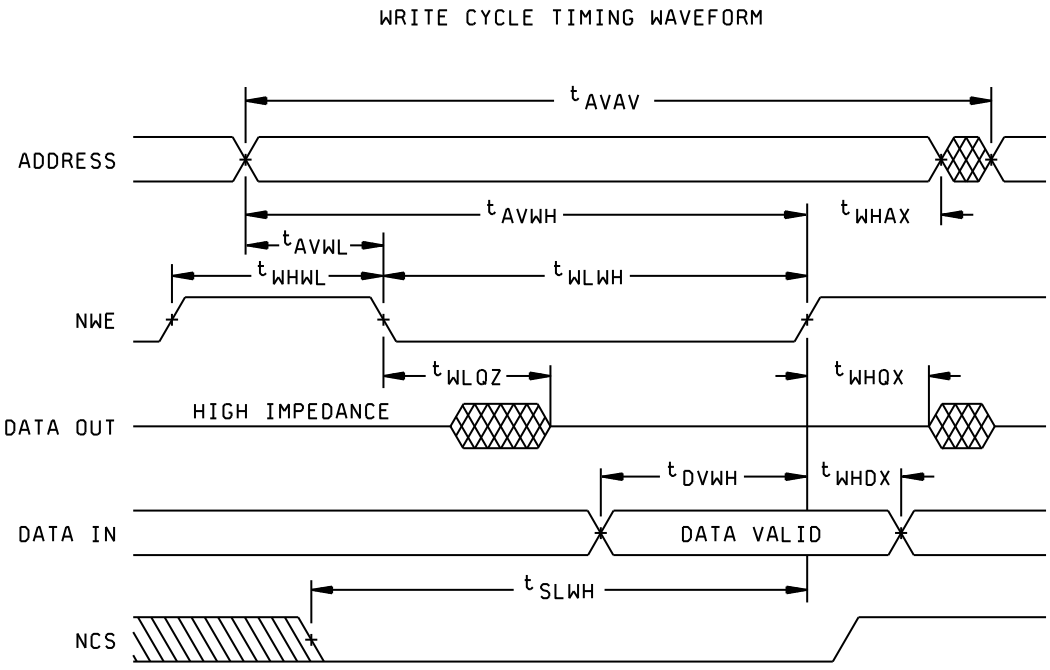


FIGURE 5. Timing waveforms - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25ºC ±5ºC, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.6 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25ºC $\pm$ 5ºC

4.4.4.2 Dose rate induced latch-up testing(survivability test). When specified by the procuring activity, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein (see 1.6). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate induced upset testing. When specified by the procuring activity, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein (see 1.6).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices (see 1.6 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM Standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0° \leq$ angled ≤ 60 degrees). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25ºC and the maximum rated operating temperature +125ºC.

f. Bias conditions shall be V_{DD} = 1.65 V dc for the upset measurements and V_{DD} = 1.95 V dc for the latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits see table IB herein.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
2	Static burn-in I and II (method 1015)	Required	Required
3	Same as line 1	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 Δ
6	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
7	Group C end-point electrical parameters	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
8	Group D end-point electrical parameters	1, 7, 9	1, 7, 9
9	Group E end-point electrical parameters	1, 7, 9	1, 7, 9

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.
7/ See 4.4.1d.

Table IIB. Delta limits. 1/ 2/

Symbol	Parameter	Delta ±
I_{DDSB}	Core Standby Current	10% of measured value or 300 µA
I_{DDDSB}	I/O Standby Current	10% of measured value or 100 µA
I_{DR1}	Core Data Retention Current	10% of measured value or 2mA
I_{DR2}	I/O Data Retention Current	10% of measured value or 50 µA
I_{ILK}	Input Leakage Current	10% of measured value or .5 µA
I_{OLK}	Output Leakage Current	10% of measured value or 1.0 µA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta. The delta limit imposed is the greater of the specified values in the table.
2/ Parameter shifts are calculated at -55°C only.

4.4.4.5 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25 ºC ±5 ºC after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7 and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latchup (SEL).

APPENDIX A

Appendix A forms a part of SMD 5962- 08202

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.1.1.1 Functional Test Conditions. V_{IH} and V_{IL} levels during functional testing shall comply with the requirements of 3.2.7 herein.

A.1.1.2 Functional Test Sequence. Functional test patterns may be performed in any order.

A.2 APPLICABLE DOCUMENTS This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March Left-Right.
Step 1. Increment address from minimum to maximum writing each address with alternating data pattern (x55).
Step 2. Increment address from minimum to maximum while performing 2a and 2b
Step 2a. Read and verify an address.
Step 2b. Write the address with complement data.
Step 3. Decrement address from maximum to minimum while performing 3a, 3b, 3c, 3d
Step 3a. Read and verify an address.
Step 3b. Write the address with complement data.
Step 3c. Read and verify the address.
Step 3d. Write the address with complement data.
Step 4. Decrement address from maximum to minimum while performing 4a and 4b
Step 4a. Read and verify the address
Step 4b. Write the address with complement data
Step 5. Decrement address from maximum to minimum while performing 5a, 5b, 5c, and 5d
Step 5a. Read and verify the address
Step 5b. Write the address with complement data
Step 5c. Read and verify the address
Step 5d. Write the address with complement data
Step 6. Decrement address from maximum to minimum while performing 6a
Step 6a. Read and verify the address

A.3.3 Algorithm C (pattern 3).

A.3.3.1 Solids.

Step1. Write x00 data pattern to all addresses from minimum to maximum.
Step 2. Read and verify x00 data pattern at all addresses.
Step 3. Write xFF data pattern to all addresses from minimum to maximum.
Step 4. Read and verify xFF data pattern at all addresses.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Control Signals Functional Verfication.

Each test performed independently.
NOE Functional test: Read with NOE = V_{IH} and confirm high-Z outputs
NCS Functional test: Read with NCS = V_{IH} and verify high-Z outputs

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-07-27

Approved sources of supply for SMD 5962-08202 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H0820201QXC	34168	HXSR01608-AQH
5962H0820201VXC	34168	HXSR01608-AVH
5962H0820202QXC	34168	HLXSR01608-AQH
5962H0820202VXC	34168	HLXSR01608-AVH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell Inc. 12001 State Highway 55 Plymouth, MN 55441