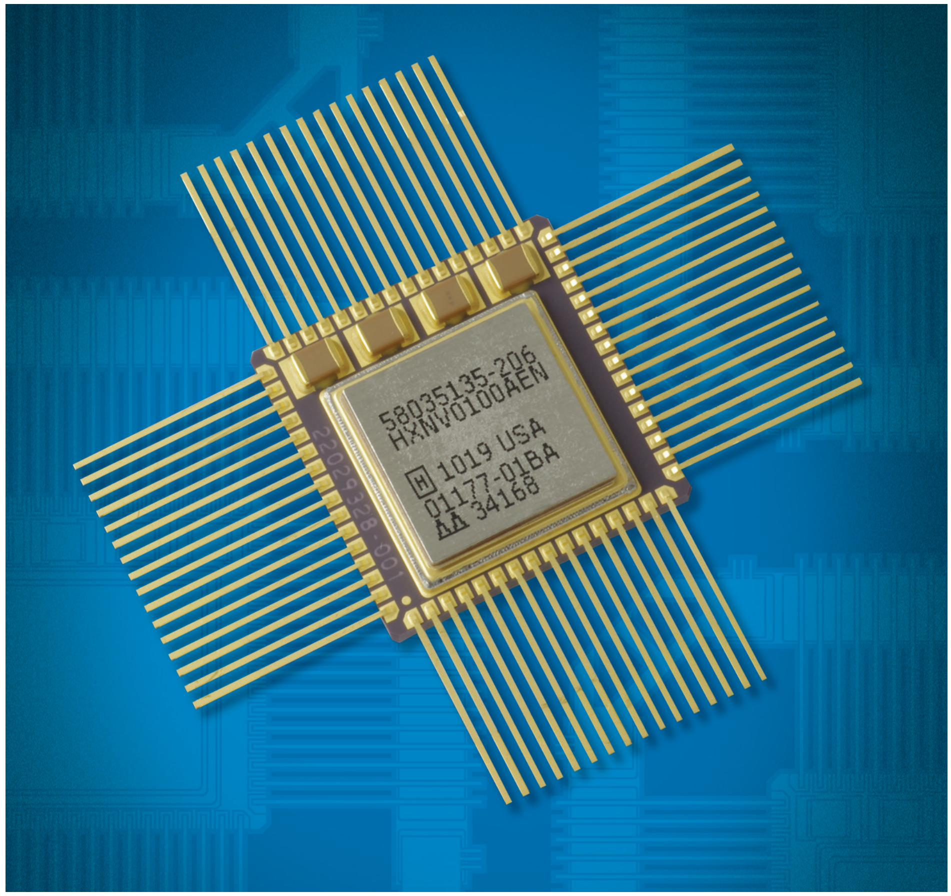
HXNV0100

Honeywell

HXNV0100 1Megabit 64K x 16 Non-Volatile Magneto-Resistive RAM

Features

- Fabricated on S150 Silicon On Insulator (SOI) CMOS Underlayer Technology
- 150 nm Process
- Total Dose Hardness $3x10^5$ and $1x10^6$ rad (Si)
- Dose Rate Upset Hardness $1x10^9$ rad(Si)/s
- Dose Rate Survivability $1x10^{12}$ rad(Si)/s
- Soft Error Rate $1x10^{-10}$ upsets/bit-day
- Neutron Hardness $1x10^{14}$ N/cm^2
- No Latchup
- Read Access Time 80 ns
- Read Cycle Time 110 ns
- Write Cycle Time 140 ns
- Unlimited Read (> $1x10^{15}$ Cycles)
- 15 years Data Retention
- Synchronous Operation
- Single-Bit Error Detection & Correction (ECC)
- Dual Power Supplies
- 1.8 V ± 0.15V, 3.3 V ± 0.3V
- 3.3V CMOS Compatible I/O
- Standard Operating Temperature Range is -40°C to +105°C
- Package: 64 Lead Shielded Ceramic Quad Flat Pack

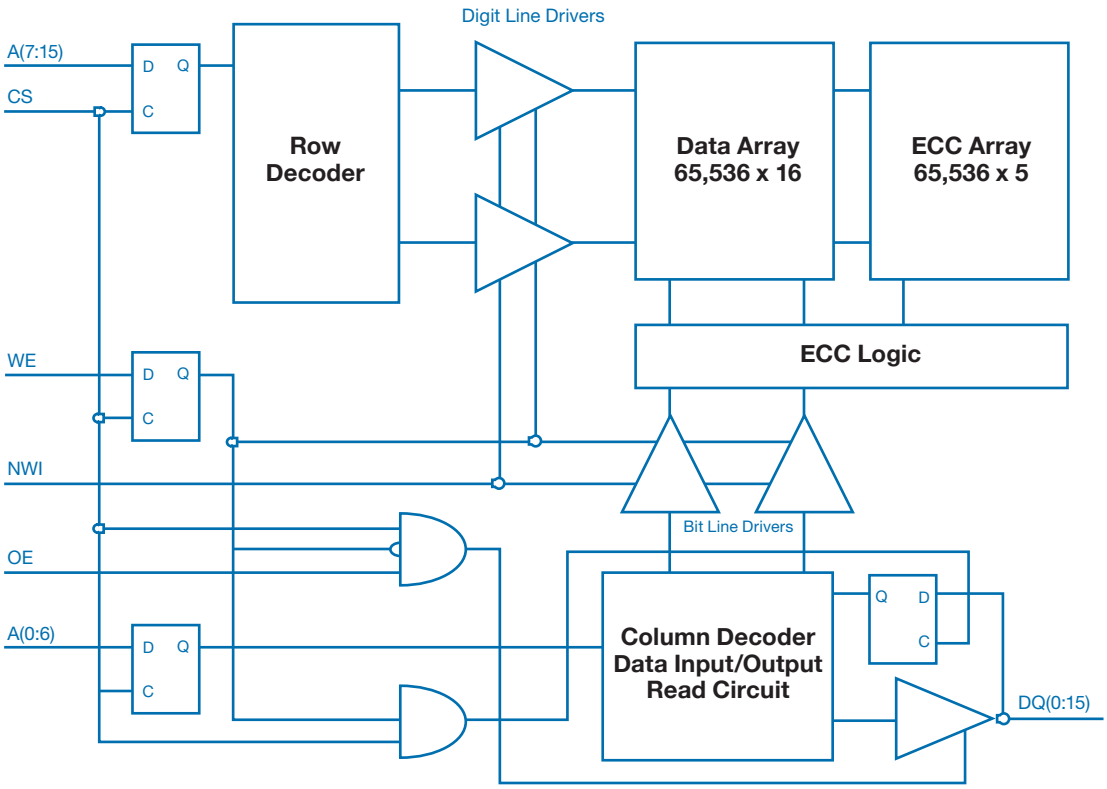


The Honeywell 1 Megabit radiation hardened low power non-volatile Magneto-Resistive Random Access Memory (MRAM) offers high performance and is designed for space and military applications. The part is configured as a 65,536 word x 16 bit MRAM.

The MRAM is designed for very high reliability. Redundant write control lines, error correction coding and low-voltage write protection ensure the correct operation of the memory and protection from inadvertent writes.

Integrated Power Up and Power Down circuitry controls the condition of the device during power transitions. It is fabricated with Honeywell's radiation hardened Silicon On Insulator (SOI) technology, and is designed for use in low-voltage systems operating in radiation environments. The MRAM operates over a temperature range of -40°C to +105°C and is operated with 3.3 ± 0.3V and 1.8 ± 0.15V power supplies.

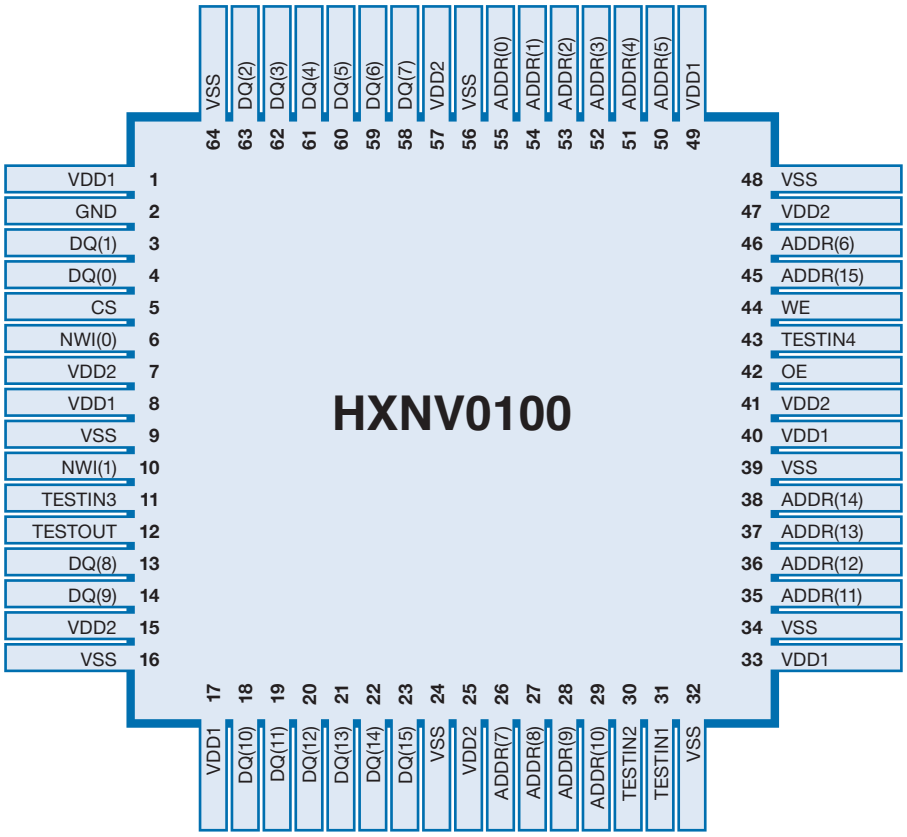
Simplified Functional Block Diagram



Signal Description

Signal	Definition
A(15:0)	A(15) is MSB, A(0) is LSB.
DQ(15:0)	Data Input/Output Signals. Bi-directional data pins which serve as data outputs during a read operation and as data inputs during a write operation.
CS	Chip select. Rising edge initiates an access of memory. A(15:0), WE and DQ(15:0) are latched on the rising edge. High level required for DQ(15:0) outputs to be enabled.
WE	Write Enable. Active high write enable. High state at rising edge of CS initiates a write cycle. Low state at rising edge of CS initiates a read cycle.
OE	Output Enable. Active high output enable. Low state puts outputs in high impedance state.
NWI0	Not Write Inhibit – When set low, these signals inhibit writes to the memory. A high level allows the memory to be written.
NWI1	NWI0 controls lower order 32K A(15)=0. NWI1 controls the upper order 32K A(15)=1. (Note the VIL and VIH requirements for NWI)
TESTOUT	This pin shall be treated as a “no connect” and have no connection on the circuit board.
TESTIN1 TESTIN2 TESTIN3 TESTIN4	These signals are for Honeywell test purposes only. These must be grounded. (Failure to hold these pins low may result in permanent loss of functionality)
VDD1	DC Power Source Input: nominal 1.8V
VDD2	DC Power Source Input: nominal 3.3V

Package Pinout



Function Truth Table

NWI	CS	WE	Function
1	R	1	Write Cycle
X	R	0	Read Cycle
0	R	1	Write Inhibited

Output Driver Truth Table

Function	CS	OE	Data Outputs
Read Cycle	1	1	Active
Read Cycle	1	0	Hi-Z
Read Cycle	0	X	Hi-Z
Write Cycle	X	X	Hi-Z
Write Inhibited	X	X	Hi-Z

RAM and ROM Functional Capability

This MRAM incorporates two write control signals allowing the two sections of the memory to be controlled independently. The two NOT WRITE INHIBIT signals, NWI(0) and NWI(1), allow one section of the device to operate as a RAM and the other to operate as a ROM at the full control of the user. These signals should be hard wired to VDD2 or ground if active control is not needed. If control is desired, maximum 5K ohms pull up or down resistor should be used with care taken to insure that the VIH and VIL for the NWI pins are met.

SOI CMOS and Magnetic Memory Technology

Honeywell's S150 Silicon On Insulator (SOI) CMOS is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques. The S150 150 nm SOI CMOS process is a technology supporting 1.8 V and 3.3 V transistors. The memory element is a magnetic tunnel junction (MTJ) that is non-volatile and composed of a magnetic storage layer structure and a magnetic pinned layer structure separated by an insulating tunnel barrier. During a write cycle, the storage layer is written by the application of two orthogonal currents using row-and-column addressing. The resistance of the MTJ depends on the magnetic state of the storage layer structure, which uses the pinned layer structure as a reference, and which enables non-destructive signal sensing, amplification, and readback. The resistance change from the memory element is a result of the change in Tunneling Magneto-Resistance (TMR) in the MTJ that depends on the magnetic state of the storage layer.

Error Correction Code (ECC)

Hamming 5-Bit ECC

A 5-bit Hamming ECC is generated for all data written into memory. This code allows for the detection and correction of all single-bit errors per address. On a read cycle, a data word is read from memory and corrected, if necessary, before being placed on the output data bus.

There is no change made to the actual data in the memory cells based on the ECC results. Actual data in memory are changed only upon writing new values.

Radiation Characteristics

Total Ionizing Radiation Dose

The MRAM has a radiation hardness assurance TID level of 300 Krad(Si) and 1Mrad(Si), including overdose and accelerated annealing per MIL-STD-883 Method 1019. Total dose hardness is assured by qualification testing with a ^{60}Co source and wafer level X-ray testing during manufacturing.

Soft Error Rate

Special process, cell, circuit and layout design considerations are included in the MRAM to minimize the impact of heavy ion and proton radiation and achieve a very low radiation induced Soft Error Rate (SER). Weibull parameters and other relevant attributes are available upon request to calculate projected upset rate performance for other orbits and environments.

Transient Pulse Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with the transient dose events. This allows the MRAM to be capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse, up to the specified transient dose rate upset specification.

The MRAM will also meet functional and electrical specifications after exposure to a radiation pulse up to the transient dose rate survivability specification.

Neutron Radiation

SOI CMOS is inherently tolerant of neutron radiation. The MRAM meets functional and timing specifications after exposure to the specified neutron fluence, based on conventional neutron irradiation testing, on unpowered MRAM parts.

Latchup

The MRAM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SOI CMOS substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. attributes are available upon request to calculate projected upset rate performance for other orbits and environments.

Radiation-Hardness Ratings (1)

Parameter	Limits	Units	Environment Conditions
Total Dose: H-Level	1×10^6	Rads(Si)	
F-Level	3×10^5		
I Soft Error Rate (2):	1×10^{-10}	Upsets/bit-day (1)	Geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield
Transient Dose Rate Upset	1×10^9	Rads(Si)/s	Pulse Width ≤ 20nS
Transient Dose Rate Survivability	1×10^{12}	Rads(Si)/s	Pulse Width ≤ 20nS
Neutron Fluence	$1x10^{14}$	N/cm^2	1 MeV equivalent energy

(1) Device will not latchup when exposed to any of the specified radiation environments.
(2) Calculated using CREME96.

Magnetic Field Characteristics

The MRAM will meet all stated functional and electrical specifications over the entire operating temperature range when exposed to magnetic fields up to the rating supplied below. Exposure to larger magnetic fields may permanently affect functionality.

Magnetic Field Rating (1)

Parameter	Limits	Units
Magnetic Field	50	Oe

(1) Tested at 25°C

Recommended Operating Conditions (1)(2)

Symbol	Parameter	Limits Min	Typical	Max	Units
VDD1	Positive Supply Voltage	1.65	1.80	1.95	Volts
VDD2	Positive Supply Voltage	3.0	3.3	3.6	Volts
T_C	External Package Temperature	-40	25	105	°C
V_{PIN}	Voltage On Any Pin	-0.3		VDD2+0.3	Volts
T_{STORE}	Storage Temperature	-55	25	105	°C

(1) Voltages referenced to GND
(2) Specifications listed in datasheet apply when operated under the Recommended Operating Conditions unless otherwise specified.

Absolute Maximum Ratings (1)

Symbol	Parameter	Ratings Min	Max	Units
VDD1	Positive Supply Voltage (2)	-0.5	2.5	Volts
VDD2	Positive Supply Voltage (2)	-0.5	4.6	Volts
V_{PIN}	Voltage on Any Pin (2)	-0.5	VDD2+ 0.5	Volts
T_{Exp}	Maximum Junction Temperature for Sustained Exposure		125 (6)	°C
T_{SOLDER}	Soldering Temperature		260°C	°C *sec(5)
P_D	Package Power Dissipation (3)		2.5	W
P_{JC}	Package Thermal Resistance (Junction to Case)		4.0	°C /W
V_{PROT}	Electrostatic Discharge Protection Voltage (Human Body Model)	2000		V
T_J	Junction Temperature Silicon		175	°C
T_{MTJ}	MTJ Temperature		160	°C
I_{OUT}	Max Output Current (7)		90	mA

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS
(3) MRAM power dissipation due to IDDS, IDDOP, and IDDSEI, plus MRAM output driver power dissipation due to external loading must not exceed this specification
(4) Not applicable.
(5) Maximum soldering temp of 250°C can be maintained for no more than 180 seconds over the lifetime of the part.
(6) Not to exceed 24 hours duration (or equivalent at temperature using Ea = 1.235 eV)
(7) Not to exceed 1 second

Capacitance (1)

Symbol	Parameter	Limit Max	Units
C_{IO}	Data I/O Capacitance	15	pF
C_I	Input Capacitance	12	pF
$C_{NWI(0),(1)}$	Not Write Inhibit Capacitance	100	pF

(1) Maximum capacitance is verified as part of initial qualification only.

DC Electrical Characteristics

Parameter	Symbol	Min	Max	Units	Comments
VIL	Low Level Input Voltage		0.3*VDD2	V	All inputs except NWI
VIH	High-level Input Voltage	0.7*VDD2		V	All inputs except NWI
VIL (NWI)	Low Level Input Voltage (NWI Signals)		0.5	V	NWI Inputs
VIH (NWI)	High-level Input Voltage (NWI Signals)	0.9*VDD2			NWI Inputs
VOL	Low-level Output Voltage		0.5	V	IOL = 6 mA
VOH	High-level Output Voltage	VDD2-0.5		V	IOH = -6 mA
IOZ	Output Leakage Current	-100	100	µA	Chip deselected or output disabled (CS=0V, OE=0V)
II	Input Leakage Current	-10	10	µA	IIL : Vin=0V, IIH : Vin=VDD2 All inputs except TEST pins
IDDSB	Standby Current				
	VDD1 (1.95V)		12	mA	
	VDD2 (3.60V)		2	mA	
IDDOPW1	VDD1 current at 1 MHZ write frequency (frequency of CS rising edges)		15	mA	
IDDOPW7	VDD1 current at 7 MHZ write frequency (frequency of CS rising edges)		30	mA	
IDD2OPW1	VDD2 current at 1 MHZ of write frequency (frequency of CS rising edges)		30	mA	
IDD2OPW7	VDD2 current at 7 MHZ of write frequency (frequency of CS rising edges)		196	mA	
IDDOPR1	VDD1 current at 1 MHZ of read frequency (frequency of CS rising edges)		14	mA	
IDDOPR9	VDD1 current at 9 MHZ of read frequency (frequency of CS rising edges)		30	mA	
IDD2OPR1	VDD2 current at 1 MHZ of read frequency (frequency of CS rising edges)		8	mA	
IDD2OPR9	VDD2 current at 9 MHZ of read frequency (frequency of CS rising edges)		54	mA	

Data Endurance

Parameter	Ratings Min	Units
Data Read Endurance	$1x10^{15}$	Cycles
Data Write Endurance	$1x10^{15}$	Cycles

Data Retention

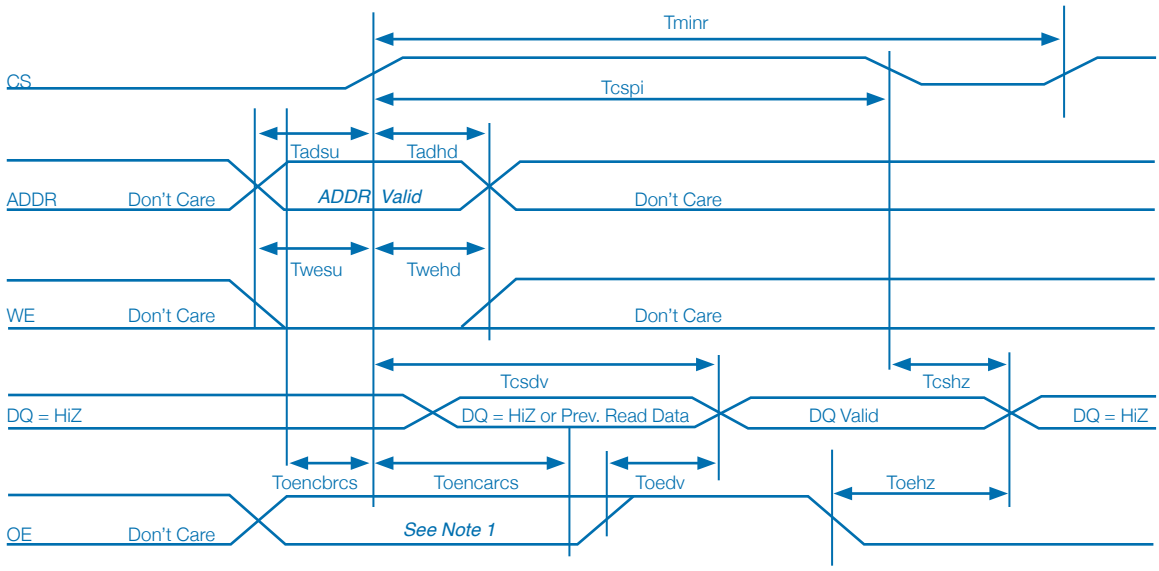
Parameter	Ratings Min	Max	Units	Conditions
Data Retention	15		years	Chip Power On or Off

Read Cycle

The MRAM is synchronous in operation relative to the rising edge of the Chip Select (CS) signal. With the initiation of a CS signal, the address and the Write Enable (WE) signal are latched into the device and the read operation begins. The memory locations are read and compared with the ECC values. Any single bit errors are detected and corrected.

If WE was low when latched in, the data word is sent to the output drivers. In addition to WE low being latched, Output Enable (OE) must be set to a high value to enable the DQ output buffers. OE is not latched, and may be set high before or after the rising edge of CS.

Read Cycle AC Timing Characteristics



(1) If OE is held high during no change window (Toencbrcs+Toencarcs), the DQ pins will drive the previously read data after rising CS.

If OE is held low during no change window, the DQ pins will remain at HiZ.

Name	Description	Min	Max	Units
TADSU	Address Setup Time	5	–	ns
TADHD	Address Hold Time	15	–	ns
TWESU	WE Setup Time	5	–	ns
TWEHD	WE Hold Time	15	–	ns
TCSDV	DQ valid with respect to rising edge of CS	–	80	ns
TOEDV	OE access time	–	15	ns
TOEHZ	OE de-asserted to outputs Hi z	–	15	ns
TCSHZ	CS de-asserted to outputs Hi z	–	20	ns
TMINR	Read Cycle Time	110	–	ns
TCSPI	CS ignored pulse width (glitch tolerance)	–	4	ns
TOENCBRCS	OE rising or falling edge to rising CS time (1)	15	–	ns
TOENCARCS	CS rising edge to OE rising or falling edge (1)	65	–	ns

(1) Guaranteed by design, not tested.
(2) The timing specifications are referenced to the Timing Input / Output References diagrams and the Timing Reference Load Circuit diagrams. IBIS models should be used to evaluate timing under application load and conditions.

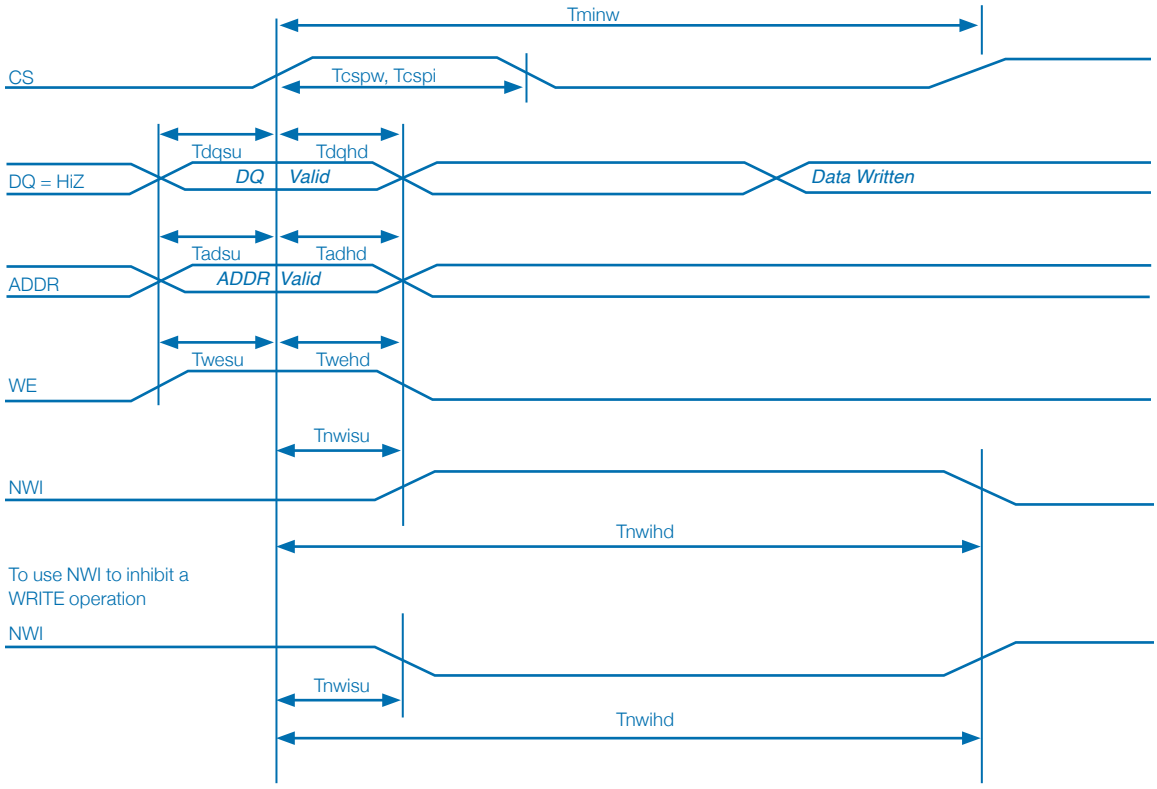
Write Cycle

The MRAM is synchronous in operation relative to the rising edge of the Chip Select (CS) signal. With the initiation of a CS signal, the address and the Write Enable (WE) signal are latched into the device.

The WRITE CYCLE begins by reading the currently addressed value in memory. The current memory data are compared to the data to be written. If the location needs to change value, the data are then written.

The bit cell construction of this device does not provide a method of simply writing a “1” or a “0” to match the data. The “write” to a bit can only change its state, thus the need to read the bit locations first. Only the bits which need to “change state” are actually written.

Write Cycle AC Timing Characteristics

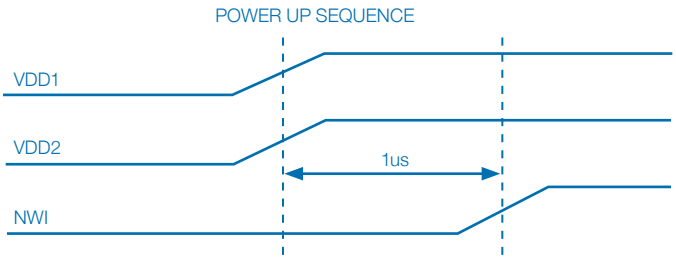


Name	Description	Min	Max	Units
TADSU	Address Setup Time	5	–	ns
TADHD	Address Hold Time	15	–	ns
TWESU	WE Setup Time	5	–	ns
TWEHD	WE Hold Time	15	–	ns
TCSPW	CS Pulse Width (for valid write)	10	–	ns
TCSPI	CS ignored pulse width (glitch tolerance)	–	4	ns
TDQSU	Data Setup Time (relative to CS rising edge)	5	–	ns
TDQHD	Data Hold Time (relative to CS rising edge)	15	–	ns
TNWISU	NWI Setup Time	-40	–	ns
TNWIHD	NWI Hold Time	140	–	ns
TMINW	Write Cycle Time	140	–	ns

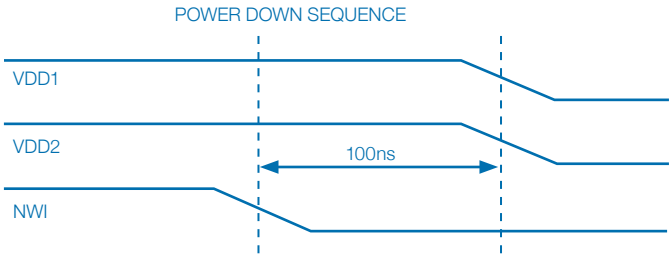
(1) The timing specifications are referenced to the Timing Input / Output References diagrams and the Timing Reference Load Circuit diagrams. IBIS models should be used to evaluate timing under application load and conditions.

Power Up Timing

During power-up there are no restrictions on which supply comes up first provided NWI is asserted (low). NWI is de-asserted within 1us of both supplies reaching their 90% values.



Power Down Timing



Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since the early 1990's. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

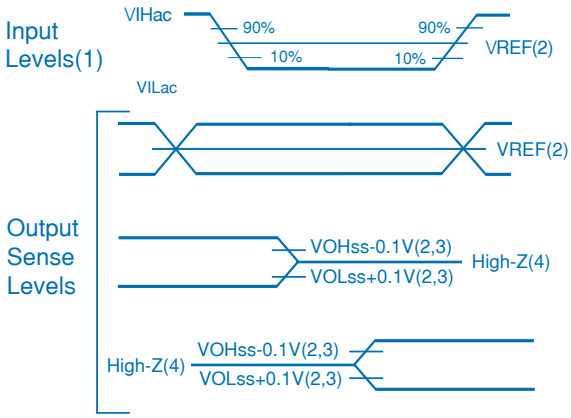
Screening and Conformance Inspection

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Conformance Summary

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package related mechanical tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

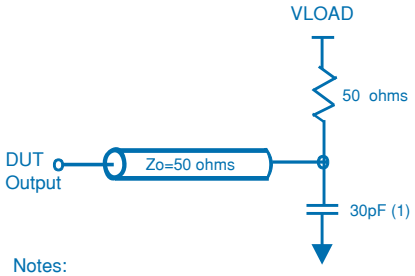
AC Timing Input and Output References



Notes:
(1) All input rise and fall times =1ns between the 90% and 10% levels.
(2) Timing parameters reference voltage level.
(3) ss: Low_Z VOH and VOL steady-state output voltage.
(4) High-Z output pin pulled to VDD2 by Output Load Circuit.

I/O Type	VIHac	VILac	VREF
3.3V CMOS	VDD2	VSS	VDD2/2

AC Timing Output Load Circuit

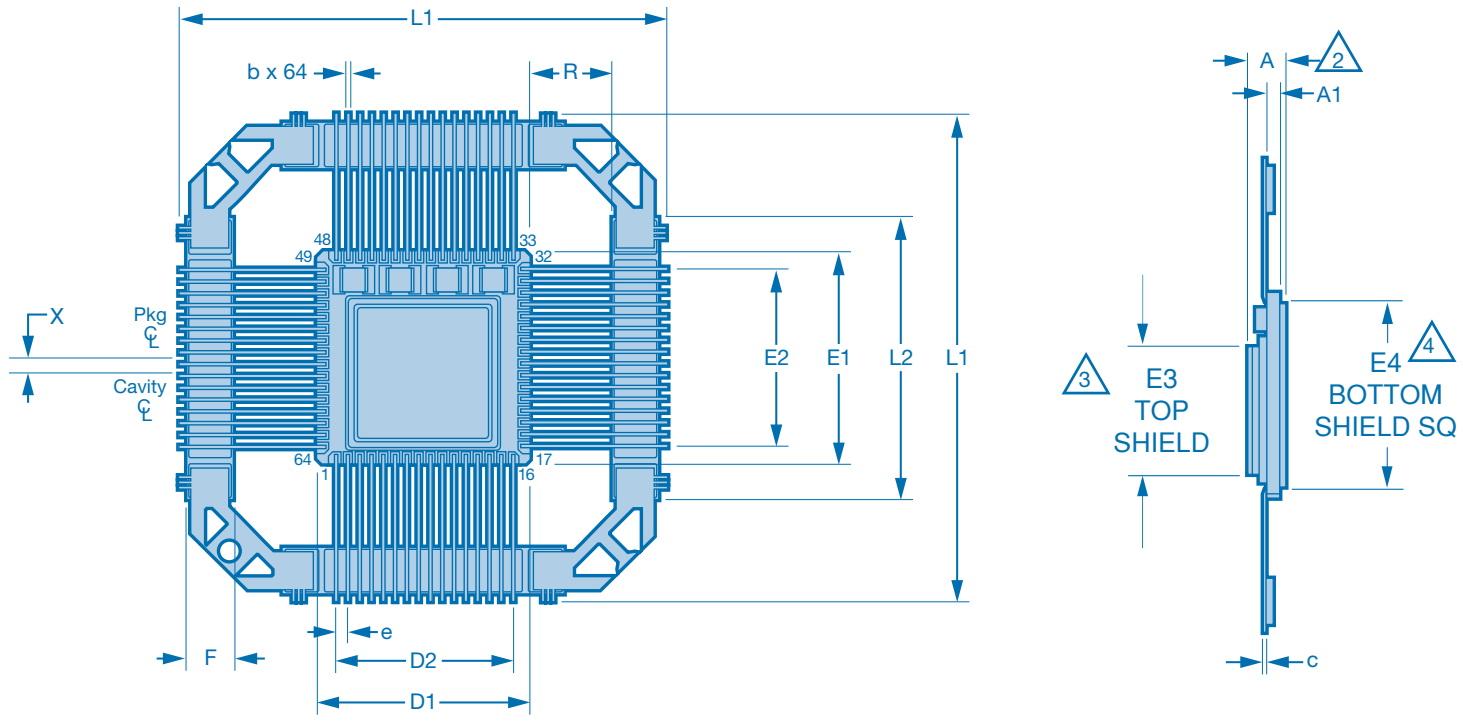


Notes:
(1) Set to 5pF for T*QZ (Low-Z to High-Z) timing parameters

I/O Type	VLOAD
3.3V CMOS	VDD2/2

Package Outline

The 64 Lead Shielded Ceramic QFP Package, including external capacitors. Magnetic shielding is tied to ground on the package.



1. Controlling dimensions are in millimeters.

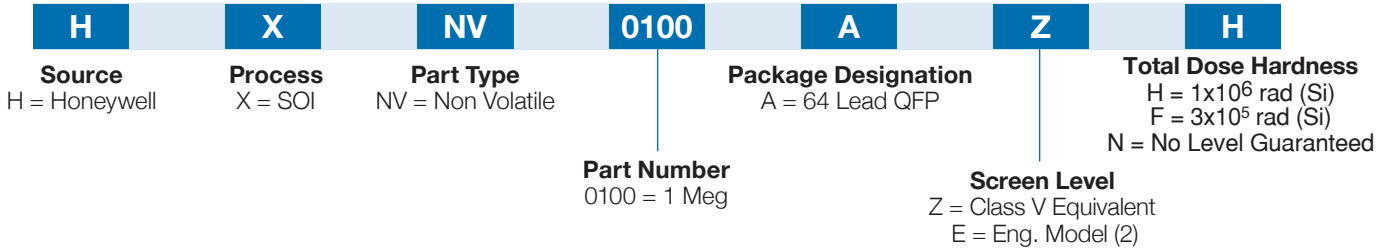
2. A is the total thickness of the top shield, lid, seal ring, ceramic body, bottom shield, and shield adhesives.

3. No edge of the shield shall extend past the outer edge of the lid flange.

4. All edges of the bottom shield shall be a minimum of 0.030" to the edge of the ceramic body.

	Common Dimensions - Millimeters			Common Dimensions - Inches		
Symbol	Min	Nom	Max	Min	Nom	Max
A	3.85	4.34	4.83	.151	.171	.190
A1	1.44	1.60	1.76	.057	.063	.070
b	0.41	0.46	0.51	.016	.018	.020
c	0.10	0.15	0.20	.004	.006	.008
D1/E1	22.63	22.86	23.09	.891	.900	.909
D2/E2	18.92	19.05	19.18	.745	.750	.755
E3	13.21	13.34	13.46	.520	.525	.530
E4	20.19	20.32	20.45	.795	.800	.805
e	1.14	1.27	1.40	.045	.050	.055
F	4.44	5.08	5.72	.175	.200	.225
L1	---	---	52.32	---	---	2.060
L2	30.10	30.48	30.86	1.185	1.200	1.215
R	8.03	---	---	.316	---	---
X	---	1.687	---	---	.066	---

Ordering Information (1)



(1) To order parts or obtain technical assistance, call 1-800-323-8295
(2) Engineering Model Description: Parameters are tested from -40°C to 105°C, 24-hour burn-in, no radiation guarantee.

QCI Testing (1)

Classification	QCI Testing
V Equivalent	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell QM Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Find out more

To learn more about Honeywell's radiation hardened integrated circuit products and technologies, visit www.honeywell.com/microelectronics.

Honeywell Aerospace
Honeywell
12001 Highway 55
Plymouth, MN 55441
Tel: 800-323-8295
www.honeywellmicroelectronics.com/

ADS-14191 Rev. B
March 2015