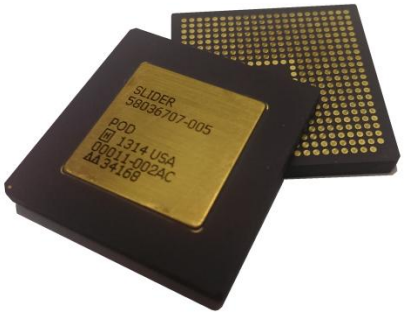
Honeywell

HXSRD02 Slider
1x/4x sRIO PHY and SERDES Quad Transceiver Radiation Hardened

The HXSRD02 Slider Integrated Circuit is a single port, four-channel, Serializer/Deserializer (SERDES) which supports data rates from 1.0 Gbps to 3.125 Gbps per lane. It is fabricated with Honeywell's 150nm silicon-on-insulator CMOS (S150) technology and is designed for use in low voltage systems operating in radiation sensitive environments. Slider operates over the full military temperature range and requires a core supply voltage of 1.8V ± 0.09V and an SSTL-2 Class I I/O supply voltage of 2.5V ± 0.2V.

Slider supports two primary operating modes. A Serial Rapid IO (sRIO) mode that supports the Physical Coding Sublayer (PCS) levels of the sRIO standard (revision 1.3). In the sRIO mode, when paired with a companion chip that handles higher levels of the sRIO protocol, Slider enables 1X/4X sRIO Endpoint or Switch functions. Slider also supports 8B/10B based, protocol-independent, SERDES communication.

On Slider, the sRIO parallel data is transmitted and received on a configurable 8-bit or 16-bit DDR or SDR SSTL-2 Class I digital interface (10-bit or 20-bit in the protocol independent mode).



When operating in the sRIO mode, Slider typically consumes 1.52W at 2.5 Gbps and 1.65W at 3.125 Gbps. For 2.5Gbps protocol-independent transceiver operation, Slider consumes a typical power of 0.48W for one channel and 1.45W for four channels. When operating at 3.125Gbps, typical power is 0.51W for one channel and 1.56W for four channels.

Slider was designed as a flexible sRIO PHY device or as a general purpose SERDES. It has many programmable features which are configured by pins and/or internal registers. HXSRD02 configuration registers are controlled via a Management Data Clock/Management Data Input/Output (MDC/MDIO) software interface per clause 45 of IEEE 802.3ae.

FEATURES

- Fabricated on S150 Silicon On Insulator (SOI) CMOS
- 4 Channel (Quad) Transceiver
- Channel Data Rates to 3.125Gb/s
- 1x/4x sRIO PHY (v 1.3) by Mercury Systems™
- Protocol Independent SERDES
- Programmable Output Amplitude, Pre-Emphasis, and Equalization
- Configurable Bus Width and Clocking
- Single CMU for all SERDES Lanes
- Reference Clock: 100MHz to 160MHz (±100 ppm)
- Total Dose $3x10^5$ and $1x10^6$ rad(Si)
- Soft Error Rate
  Heavy Ion ≤$1x10^{-12}$ BER
  Proton ≤$1x10^{-12}$ BER
- Neutron $1x10^{14}$ cm^{-2}
- Dose Rate Upset $1x10^{10}$ rad(Si)/s
- Dose Rate Survivability $1x10^{12}$ rad(Si)/s
- Latch-Up Immune
- Core/SERDES Power Supply 1.8 V ± 0.09 V
- SSTL-2 Class I Parallel Interface 2.5 V ± 0.2 V
- Operating Temperature Range -55°C to +125°C
- 467 Lead Ceramic Land Grid Array (LGA)
- 15 Year Lifespan Across All Temperatures
- SMD: 5962-14224 - pending

HXSRD02

GENERAL DESCRIPTION

HXSRD02, or Slider, is an integrated circuit containing four SERializer/DESerializer (SERDES) lanes configured as a single port with four independent full-duplex lanes.
Slider can be used as a 1x/4x sRIO PHY (v 1.3) or as protocol-independent general purpose SERDES.
The parallel interface is clocked at 1/10 or 1/20 of the SERDES line rate. The parallel interface is configurable in both bus width and data clocking mode, single data rate (SDR) and dual data rate (DDR).
A single Clock Multiplier Unit (CMU) is used for the entire integrated circuit to provide a multiplied reference clock to each channel. The configuration registers are controlled via a Management Data Clock/Management Data Input/Output (MDC/MDIO) software interface per clause 45 of IEEE 802.3ae.

Protocol Support

- 1x/4x sRIO PHY (v 1.3)
  - Enables Endpoint/Switch function when paired with Mercury Systems™ IP in companion IC
- Protocol Independent or Protocol Bypass SERDES
  - Passes 8b10b encoded serial data (data encoded and decoded external to Slider)
  - Can be used for any 8b10b encoded protocol, such as: 1GE, 1/2G FC, 10GE (XAUI), 10GFC (XAUI)

Transmitter Features

- Conversion from parallel to serial data and multiply data rate
- Transmit 8b10b encoder (in sRIO mode only)
- Ability to independently power down any transmit lanes
- Ability to independently disable high-speed output buffers
- Programmable transmitter with pre-emphasis and output signal amplitude

Receiver Features

- Four independent Clock and Data Recovery (CDR) circuits
- Programmable receiver equalization
- Programmable receiver loss of signal detection
- On-chip, 100Ω resistor termination
- Designed for an AC-coupled serial interface
- Receive byte alignment and 8b10b decoder (in sRIO mode only)
- 1x/4x sRIO lane to lane de-skewing (trunking) and clock offset (clock skew) compensation

Miscellaneous Features

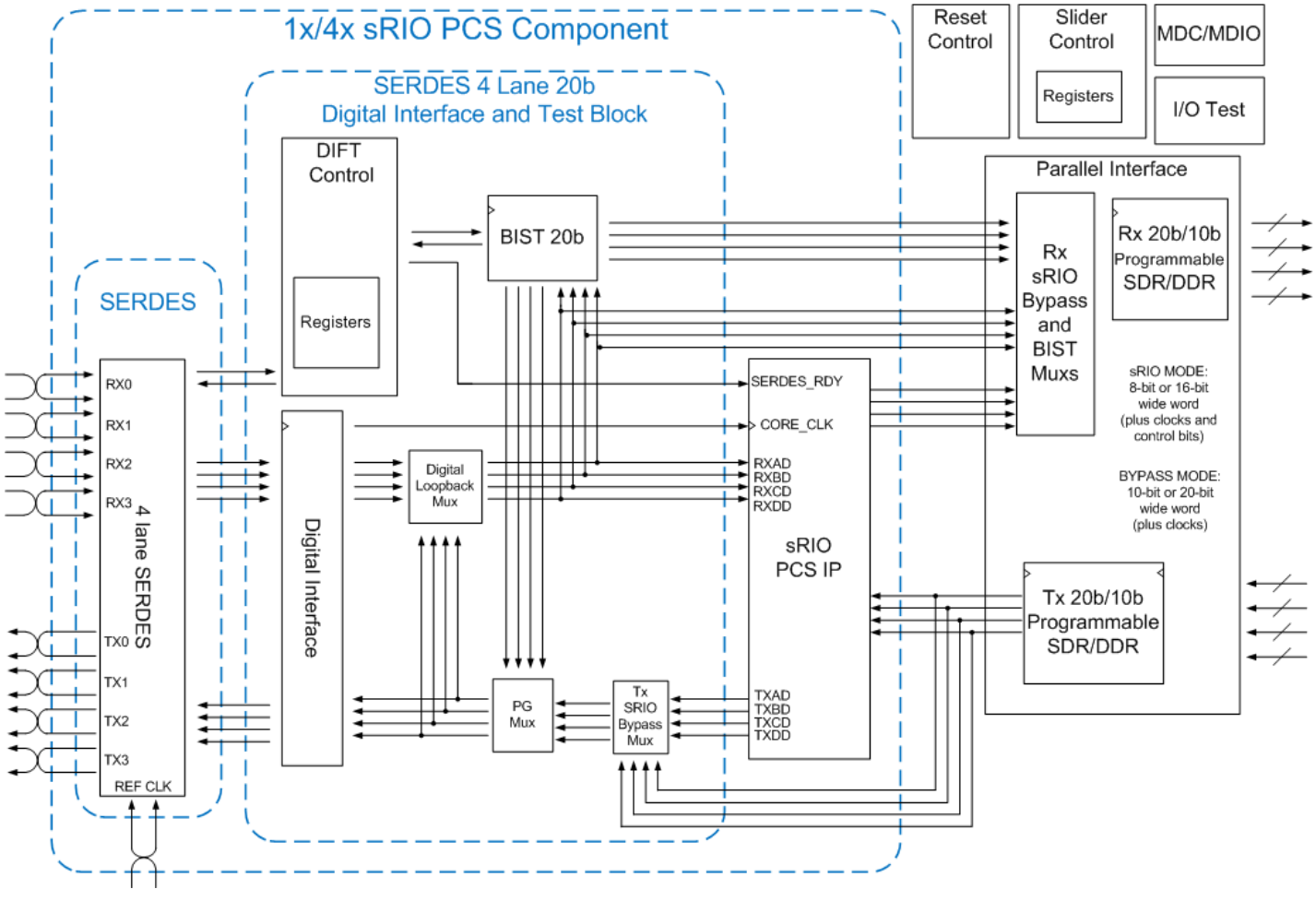
- One integrated CMU is used to provide a high speed clock for all four SERDES lanes
- Parallel SSTL-2 Class I data interface (sRIO mode) is: four lanes of 8-bit or 16-bit data and protocol side-band signals, SDR or DDR
- Parallel SSTL-2 Class I data interface (protocol independent mode) is: four lanes of 10-bit or 20-bit data, SDR or DDR
- Integrated pattern generator including 9 built-in patterns and user defined pattern capability
- Internal pattern comparator circuitry for Built In Self Test (BIST) and at-speed diagnostics
- Three integrated data loopback modes to support “at speed” testing.

APPLICABLE DOCUMENTS

This document is a high level description of the general operation, features, functions, and protocol support. See the HXSRD02 Slider User’s Guide for complete detailed operation.

- HXSRD02 Slider User’s Guide – Detailed information regarding features and operation.
- HXSRD02 Register Description – Detailed description of all the registers.

SIMPLIFIED FUNCTIONAL DIAGRAM



CONFIGURATION CONTROL AND PROGRAMMING

Slider is primarily configured via pin settings upon power-up. In addition to the pins, Slider's settings can be changed or modified via registers. The device includes a two wire serial management interface for register access. The interface supports MDC/MDIO interface per clause 45 of IEEE 802.3ae. The MDC/MDIO interface supports access at 2.5 MHz with indirect addressing per the IEEE specifications.

DATA COMMUNICATION PROTOCOL

Slider can be configured either as a sRIO PCS PHY or as a protocol independent SERDES in the bypass mode.

When in sRIO mode, Slider is configured to be a SERDES PHY component. A PHY is a single (10Gpbs), 1X/4X SERDES port and Physical Coding Sublayer (PCS). The sRIO PCS layer was provided by Mercury Systems™. The PCS layer supports Mercury's sRIO Endpoint applications (revisions 1.2, 1.3, 2.0-2.3, and 3.0) through the use of Slider and a second device. Consult Mercury Systems™ for sRIO Endpoint details.

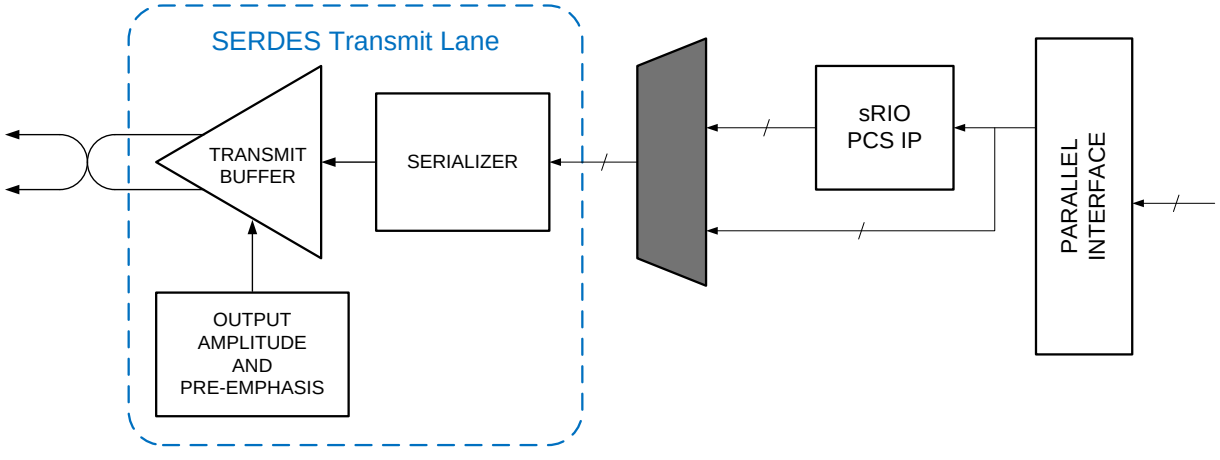
In the protocol bypass or protocol independent mode, Slider simply serializes and/or de-serializes raw 8b10b encoded data. In this mode, no byte alignment or 8b10 encoding or decoding is performed in the device.

SERDES OPERATION

Within Slider is a 4-lane Serializer/Deserializer (SERDES). A SERDES converts an 8b10b encoded parallel word to serial data in a transmit lane or converts serial data to 8b10b encoded parallel word in a receive lane. In Slider this 8b10b encoded data is passed between the sRIO logic and the SERDES internal to Slider in the sRIO mode. In protocol bypass mode, the 8b10b encoded data is passed directly between the parallel interface and the SERDES.

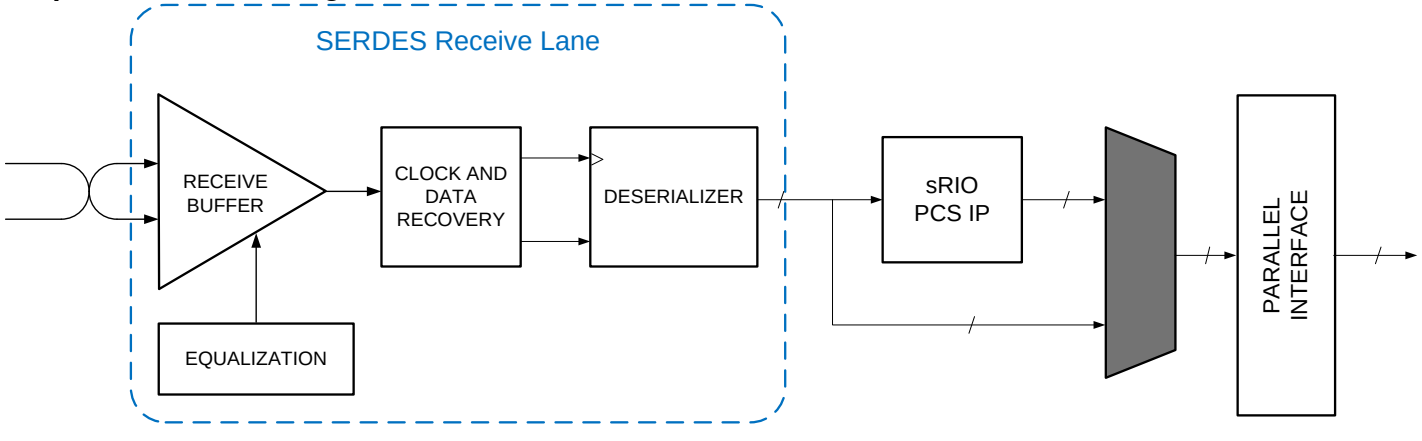
The high speed serial interface has a total of 4 lanes, each consisting of a transmitter and receiver. The data rates for each lane range from 1 Gbps to 3.125 Gbps. For sRIO 4x applications, the data for the 4 lanes is grouped and aligned within Slider. Each lane can be controlled independently including on/off control, data rate, signal levels, pre-emphasis, and equalization.

Simplified Transmitter Diagram



Each transmit lane receives 8b10b encoded from either the sRIO logic or the parallel interface. This data is serialized and transmitted. The transmit buffer includes internal 100Ω differential termination resistance, and is designed to drive an AC coupled channel.

Simplified Receiver Diagram



Each receive lane receives data through a high speed differential serial receiver. The Clock and Data Recovery block (CDR) recovers the clock from the incoming 8b10b encoded data stream. The high speed serial data is then be de-serialized into a 10-bit, unaligned word. This 10-bit word is then passed to the sRIO logic or directly to the parallel interface depending on the operating mode. The receive buffer includes internal 100Ω differential termination resistance, and is designed to be driven from an AC coupled channel.

Clock Multiplier Unit (CMU)

The single Clock Multiplier Unit (CMU) generates high frequency clocks by multiplying the reference clock. The multiplication factor can be set to 10 or 20. The data rate is controlled by the reference clock, CMU multiplication factor, and rate selection. In sRIO modes, all lanes will have identical data rates. In the protocol bypass mode, different rates could be selected for each of the four lanes. The CMU also generates the clocks used throughout the chip.

The reference clock going into the CMU must be the same as the clock for the parallel port transmit data coming into Slider (0 ppm difference). There is no clock compensation on the transmit path in sRIO mode. In the protocol bypass mode, there is no clock compensation on either the transmit or the receiver path.

Reference Clock Implementation

The reference clock input for Slider is an LVPECL receiver. These signals must be AC-coupled externally using 0.01 µF capacitors. These signals are internally terminated using two 100kΩ terminating resistors connected between power and ground to a common-mode point that will act as an AC ground.

Loopback Features

Slider offers several loopback features that can be used for system testing or repeater function. These loopbacks are primarily controlled by register settings via the MDC/MDIO interface.

Serial Loopback

Serial loopback provides a path from the transmit serializer to the receive clock and data recovery unit. The transmit buffer will continue to transmit data from the serializer while in serial loopback mode. When in serial loopback mode, the data from the serial receive buffer is ignored. This path is differential and can be used at data rates up to 3.125 Gbps.

Metallic Loopback

Metallic loopback provides a path from the serial differential receive buffer to the serial differential transmit buffer. This loopback feature essentially re-amplifies the received signal. This path is single ended and is intended for data rates below 2 Gbps (1 GHz). Pre-emphasis is not available in metallic loopback mode. If a lane is in metallic loopback mode, the data from the transmit serializer is ignored by the transmit buffer.

Parallel Loopback

In parallel loopback the parallel data is looped at the parallel interface. The serial receive data is deserialized and then internally routed to the parallel section of the transmitter. It is then reserialized and transmitted out the serial transmit path. In this mode, the part must be in protocol bypass mode. Parallel loopback along with the protocol bypass mode enables re-amplification and pre-emphasis of the data. Note that clock compensation is defined at the protocol level. In protocol bypass mode, Slider provides no clock mismatch compensation. For complete retimer or repeater capabilities, a companion device would be required.

SERDES SERIAL RECEIVER INPUTS AND TRANSMITTER OUTPUTS CHARACTERISTICS

The SERDES transmitter is internally 100Ω terminated and is designed to drive an AC-coupled load. It has a common mode voltage at approximately 0.9V. The output amplitude is programmable from 600 to 1400 mV (differential peak-to-peak) in 200 mV increments. Typical rise and fall times (20% to 80%) are 90 ps into a 100Ω load (rise and fall times are dependent on the load and media characteristics). In addition, the transmitter has seven register-programmable pre-emphasis settings to compensate for lossy systems.

Transmitter Jitter Characteristics (1)

Jitter Type	Data Rate	Value (in Unit Intervals)
Total Jitter	1.25 Gbps	0.23
	2.125 Gbps	0.33
	3.125 Gbps	0.35
Deterministic Jitter	1.25 Gbps	0.11
	2.125 Gbps	0.20
	3.125 Gbps	0.17

Notes:
(1) These values represent approximate worst case jitter values. Jitter has a strong dependency on a number of system characteristics such as the reference clock jitter and power supply noise.

The SERDES receiver is also internally 100-ohm terminated and is required to be AC-coupled from the transmitter. The receiver sets its own internal common mode voltage. The receiver has programmable equalization to re-amplify higher frequency signal loss. It also has programmable loss of signal detection.

Receiver Jitter Tolerance Characteristics (1)

Jitter Type	Data Rate	Value (in Unit Intervals)
Total Jitter Tolerance (includes 0.1 UI Sinusoidal Jitter)	1.25 Gbps	0.68
	2.125 Gbps	0.62
	3.125 Gbps	0.65
Deterministic Jitter Tolerance	1.25 Gbps	0.33
	2.125 Gbps	0.37
	3.125 Gbps	0.37

Notes:
(1) These values represent approximate worst case jitter values. Jitter has a strong dependency on a number of system characteristics such as the reference clock jitter and power supply noise.

PARALLEL PORT INTERFACE

The parallel interface operates on the 2.5 V domain with SSTL-2 Class I I/O. The bus width and clocking of the parallel interface is programmable to allow for flexibility when integrating with a second device. The bit width can be configured as either a DDR “short word” or as a SDR or DDR “wide word.” The bus width on the parallel interface is independent of the serial data rate.

In the “short word” configuration, the byte width is 8 bits wide in the sRIO mode and 10 bits wide in the protocol bypass mode. The data in this configuration must be clocked in the DDR mode. This configuration allows for lower pin counts on the parallel interface. The parallel data rate for “short word” is twice that of the “wide word” data rate for equal throughput.

In the “wide word” configuration, the byte width is 16 bits wide in the sRIO mode and 20 bits wide in the protocol bypass mode. In this configuration, the data can be clocked in either DDR or SDR modes. This configuration is for systems that require a lower speed parallel interface.

In addition to the data bits in the sRIO mode, there are a protocol side-band signals for control and status bits as defined by the sRIO protocol. These sRIO signals are explained in further detail in the user’s guide. In a “wide word” protocol bypass mode, these side-band signals are utilized as data bits to increase the bus width from 16 to 20 bits.

The device driving the parallel data into the transmitter parallel interface of Slider must be the same frequency as the SERDES input reference clock on Slider (0 ppm difference). In sRIO mode, there is no clock compensation on the transmit path. In the protocol bypass mode, there is no clock compensation on either the transmit or the receiver path.

TYPICAL POWER CONSUMPTION CHARACTERISTICS

These are the typical power number for several different device configurations at both 2.5 Gbps and 3.125 Gbps. Extrapolation can be used to estimate power at different speeds. Typical power is at nominal voltage and 25°C.

Both the analog SERDES (VDDA) and the core logic (VDD) are powered from a 1.8V supply.

The parallel I/O supply (VDD2) is a 2.5 supply. The power numbers listed are for a “wide-word,” SDR configuration. In SRIO mode, “wide-word” means 16-bit wide word plus the protocol control signals and clocks. The SRIO power numbers are given assuming all four transmit and receive lanes are operational (SRIO 4x mode). In the protocol bypass mode, “wide-word” means 20-bit wide word plus clocks. The power numbers are given for several different combinations of operational lanes. The SSTL-2 Class I I/O are terminated with 50Ω resistors to VDD2 / 2.

Slider Configuration	Active Lanes Transmit / Receive	Data Rate (Gbps)	VDDA 1.8 V (mW)	VDD 1.8 V (mW)	VDD2 2.5 V (mW)
4X SRIO Mode	4 TX / 4 RX	2.5	670	244	610
		3.125	695	287	670
Protocol Bypass	4 TX / 4 RX	2.5	670	168	610
		3.125	695	198	670
	1 TX / 1 RX	2.5	274	50	152
		3.125	286	58	167
	4 TX / 0 RX	2.5	344	74	345
		3.125	365	87	377
	1 TX / 0 RX	2.5	192	26	86
		3.125	204	31	94
	0 TX / 4 RX	2.5	434	104	265
		3.125	440	123	293
	0 TX / 1 RX	2.5	190	34	66
		3.125	193	40	73

RADIATION CHARACTERISTICS

RADIATION-HARDNESS RATINGS (1)

Symbol	Parameter	Environment Conditions	Limits	Unit
TID	Total Ionizing Dose		H = $1x10^{6}$ F = $3x10^{5}$	rad(Si)
DRU	Transient Dose Rate Upset	Pulse width ≤20ns	$1x10^{10}$	rad(Si)/s
DRS	Transient Dose Rate Survivability	Pulse width ≤20ns	$1x10^{12}$	rad(Si)/s
SER (2)	Bit Error Ratio (3) Heavy Ion Proton	Geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield	 $<1x10^{-12}$ $<1x10^{-12}$	 BER BER
	Neutron Irradiation Damage	1 MeV equivalent energy	$1x10^{14}$	n/cm^2

(1) Device will not latchup when exposed to any of the specified radiation environments.
(2) Calculated using CREME96.
(3) The Bit Error Ratio (BER) is defined as the number of bit errors per bits sent due to ion-induced single event upset

Total Ionizing Radiation Dose

Slider's radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Transient Pulse Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with transient dose events. This enables Slider to be capable of operation during and after exposure to a transient dose rate ionizing radiation pulse, up to the DRU level listed. The device will also meet functional and timing specifications after exposure to a transient dose rate ionizing radiation pulse up the DRS level listed.

Neutron Radiation

SOI CMOS is inherently tolerant to damage from neutron irradiation. Slider meets functional and timing specifications after exposure to the specified neutron fluence.

Single Event Soft Error Rate

Slider will have a single event soft error rate contribution to the Bit Error Ratio (BER) while operating under the recommended operating conditions. Slider has a non-radiation environment specified BER of $1X10^{-12}$. This specified BER is a result of meeting the IEEE802.3, Clause 39 Total and Deterministic Jitter requirements. Special process, circuit and layout design considerations were implemented in Slider to minimize the impact of heavy ion and proton radiation and achieve small projected BER. These techniques sufficiently harden the Slider such that the contribution to BER due to single event upsets is negligible compared to the IEEE802.3 BER specification.

Latchup

Slider will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

SIMULATION MODELS

Simulation models and associated test benches are available upon request. These include:

- Encrypted HSPICE Model: High speed serial interface simulation (including package and columns)
- IBIS Model: Board level signal integrity simulation of other signal I/O (excluding the high speed serial interface)
- Verilog Model: Functional simulation of HXSRD02
- Verilog Test Benches: There are several test benches associated with the sRIO and protocol bypass modes

RELIABILITY

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

SCREENING AND CONFORMANCE INSPECTION

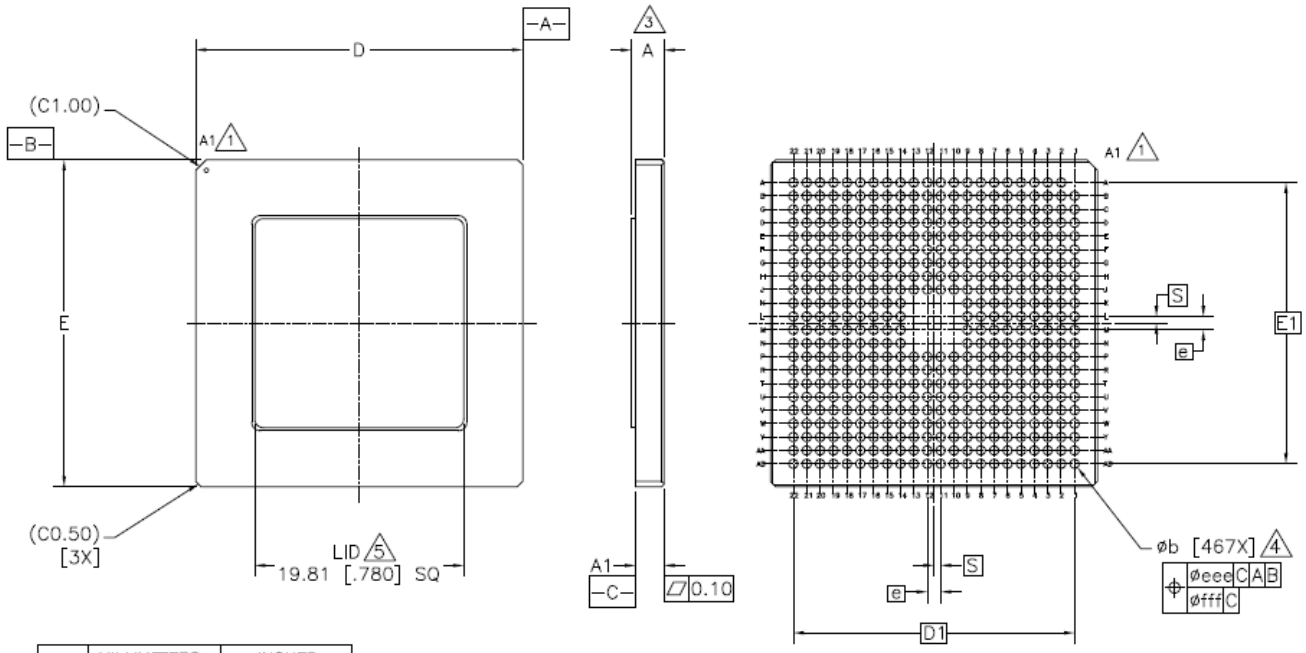
The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Conformance Summary

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests - 1000 hours at 125C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

PACKAGE OUTLINE

The package is 467-lead ceramic LGA. Pin A1 (unpopulated) is in the lower left hand corner of the package when the columns are facing down. Rows 10-13 in columns K-N are unpopulated. Solder columns are the recommended method of attaching these components to a circuit board.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.80	3.12	3.43	.110	.123	.135
A1	2.42	2.69	2.96	.095	.106	.117
b	0.81	0.86	0.91	.032	.034	.036
D E	30.80	31.00	31.20	1.213	1.220	1.228
D1 E1	26.67			1.050		
e	1.27			0.050		
S	0.635			0.025		
eee	0.30			0.012		
fff	0.15			0.006		

5. LID CENTERED ON PACKAGE.

4. b = DIAMETER OF THE METALIZED LGA PAD.

3. DISTANCE FROM BOTTOM OF THE CERAMIC TO THE TOP OF THE LID.

2. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.

1. THE A1 CORNER IS IDENTIFIED BY A LARGER CHAMFER AND A DOT ON THE TOP CERAMIC SURFACE.

HXSRD02

ORDERING INFORMATION (1)

Standard Microcircuit Drawing (SMD)

The QML qualified HXSRD02 device can be ordered under the SMD drawing 5962-14224 (pending).

Order Code

H X SRD02 T V H

SOURCE
H = Honeywell

PROCESS
X = SOI(S150)

PART NUMBER
SRD02

PACKAGE DESIGNATION
T = 467 LGA

SCREEN LEVEL
V = QML Class V - pending
W= QML Class Q (+ additional screening) – pending
Z = Class V Equivalent (3)
E = Engineering Model (2)

TOTAL DOSE HARDNESS
H = $1x10^6$ rad(Si)
F = $3x10^5$ rad(Si)
N = No Level Guaranteed (2)

(1) Orders may be faxed to 763-954-2051.
Please contact our Customer Service Representative at 763-954-2474 or 1-800-323-8295 for further information.
(2) Engineering Model Description: Screen Level and Total Dose Hardness codes must be “E” and “N” respectively. Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation hardness guaranteed.
(3) These receive the Class V screening.

FIND OUT MORE

For more information about Honeywell’s family of radiation hardened integrated circuit products and services, visit www.honeywellmicroelectronics.com.

Honeywell
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