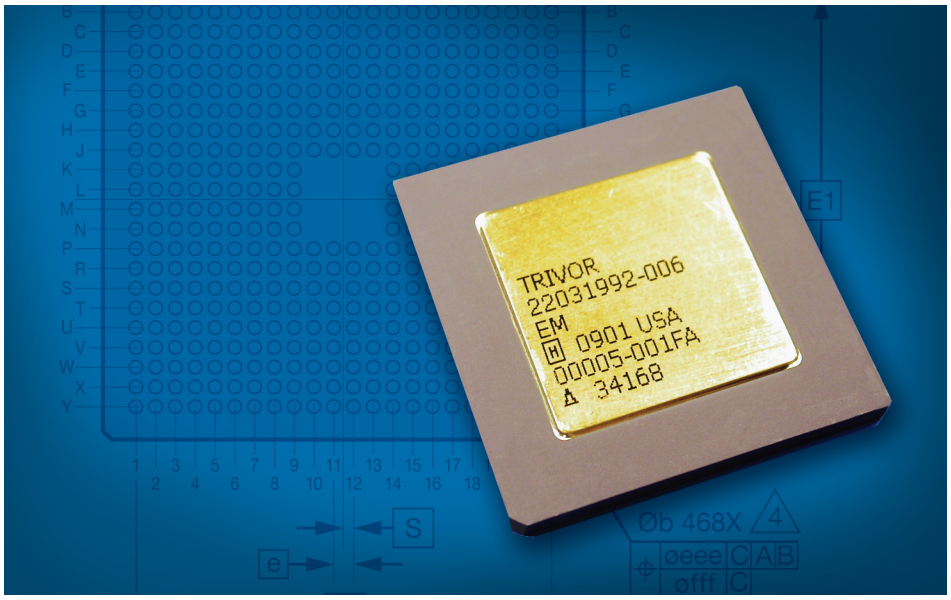
HXSRD01 Trivor

Honeywell

SERDES Quad Redundant Transceiver Radiation Hardened

Features

- Fabricated on S150 Silicon On Insulator (SOI) CMOS
- 150 nm Process (Leff = 110 nm)
- 4 Channel (Quad) Transceiver with Redundant Transmitters
- Channel Data Rates to 3.1875Gb/s
- Multi-Channel XAUI to 10Gb/s
- Supports Ethernet and Fibre Channel Protocols
- Programmable Amplitude, Pre-Emphasis, Equalization
- CMOS Compatible I/O
- Total Dose $3x10^5$ and $1x10^6$ rad(Si)
- Soft Error Rate
  Heavy Ion $\leq 1x10^{-12}$ Upsets/bit-day
  Proton $\leq 2x10^{-12}$ Upsets/bit-day
- Neutron $\geq 1x10^{14}$ cm-2
- Dose Rate Upset $\geq 1x10^{10}$ rad(Si)/s
- Dose Rate Survivability
  $\geq 1x10^{12}$ rad(Si)/s
- No Latch up
- Core Power Supply
  1.8 V ± 0.09 V
- Parallel interface bus is SSTL-2
- Operating Range is
  -55°C to +125°C
- 468 Lead Ceramic Land Grid Array (LGA) 31 x 31 mm



The HXSRD01 Trivor Serializer/Deserializer (SERDES) Integrated Circuit is a four channel, redundant SERDES which supports data rates from 1.0Gb/s to 3.1875Gb/s per lane. It is fabricated with Honeywell's 150nm silicon-on-insulator CMOS (S150) technology and is designed for use in low voltage systems operating in radiation sensitive environments.

HXSRD01 operates over the full military temperature range and requires a core supply voltage of 1.8V +/- 0.09V and an I/O supply voltage of 2.5V ± 0.2V.

It supports point to point communications and networking for 1G Ethernet, 1G and 2G Fiber Channel and 10G XAUI Ethernet and Fiber Channel communication protocols.

The Trivor contains a single Clock Multiplier Unit (CMU) which is used for the entire integrated circuit to provide a multiplied reference clock to each channel. The data is sent to Trivor in 8 bit bytes with a clock and the data is then 8b10b encoded and transmitted. The receiver will perform byte and frame alignment, clock and data recovery, 8b10b decode and output a clock and 8 bit data. The digital interface is SSTL-2.

For 1Gb/s transceiver operation, the Trivor consumes typical power of 0.53W for one channel and 1.1W with four channels. When operating at 3Gb/s, typical power is 0.9W for one channel and 1.7W for four channels.

Trivor was designed to be a flexible device and has many programmable features which are configured by internal registers. The Trivor configuration registers are controlled via a Management Data Clock/Management Data Input/Output (MDC/MDIO) software interface per clause 45 of IEEE 802.3ae.

General Description

The Trivor integrated circuit contains eight SERializer/DESerializer (SERDES) channels divided into two ports (A and B) with four full duplex lanes. Port B is the primary port and Port A is the redundant port. The receive ports are multiplexed to provide access to either port A or port B from the parallel side receive interface. The transmit ports are redundant such that data from the parallel interface is transmitted on both serial ports A and B. The parallel side interface provides access to the four serial lanes of de-serialized data via four 10-bit buses. A single Clock Multiplier Unit (CMU) is used for the entire integrated circuit to provide a multiplied reference clock to each channel. The Trivor configuration registers are controlled via a Management Data Clock/Management Data Input/Output (MDC/MDIO) software interface per clause 45 of IEEE 802.3ae.

Trivor supports data transmission for the following protocols and applications.

- 1G Fibre Channel – 8 TX and 8 RX lanes operating at 1.0625Gbps.
- 2G Fibre Channel – 8 TX and 8 RX lanes operating at 2.125Gbps.
- 10G Fibre Channel XAUI – 2 ports (A and B) of four lanes operating at 3.1875Gbps per lane. The lanes are trunked together consistent with 10G Fibre Channel protocol.
- 1 Gigabit Ethernet – 8 TX and 8 RX lanes operating at 1.25Gbps.
- 10 Gigabit Ethernet XAUI – 2 ports (A and B) of four lanes operating at 3.125Gbps per lane. The lanes are trunked together consistent with 10G Ethernet protocol.
- General backplane applications between 1.0625 and 3.1875 Gbps utilizing either Fibre Channel or Gigabit Ethernet protocols.

Transmitter Features

- Interface to four lanes of 8 bit, parallel data via SSTL-2 bus, SDR or DDR
- Conversion from parallel to serial data and multiply data rate
- Transmit 8b10b encoding
- Ability to independently power down any transmit lanes
- Ability to independently disable high-speed output buffers
- Integrated Pattern Generator including 15 patterns
- Programmable transmitter with pre-emphasis and output signal amplitude
- Redundant Data Transmission – Same data transmitted on channels of Port A and Port B

Receiver Features

- Eight independent Clock and Data Recovery (CDR) circuits
- Programmable receiver equalization
- Programmable receiver loss of signal detection
- On-chip, 100-ohm resistor termination
- Designed for an AC-coupled serial interface
- Receive Byte Alignment and 8b10b decode logic
- XAUI lane to lane de-skewing (trunking) and clock offset (clock skew) compensation
- Parallel interface using SSTL-2 buffers
- Supports +/- 200 ppm deviation from the line data rate to the local data rate
- Internal pattern comparator circuitry for Built In Self Test (BIST) and at-speed diagnostics
- Three integrated data loopback modes to support “at speed” testing.
- One integrated CMU is used to provide a high speed clock for all eight SERDES lanes

Protocols

- Supporting Fibre Channel operating frequencies of 1.0625 Gbps, 2.125 Gbps and 3.1875 Gbps from a common reference clock.
- Gigabit Ethernet at 1.25 Gbps.
- Supports MDC/MDIO interface per clause 45 of IEEE 802.3ae, as well as industry standard two wire serial interface for Fibre Channel applications.

Functions

- Support for XAUI lane to lane de-skewing (trunking) and clock ppm offset (clock skew) compensation.
- XGMII and FC-HSPI parallel interface using SSTL-2 buffers.

Electrical

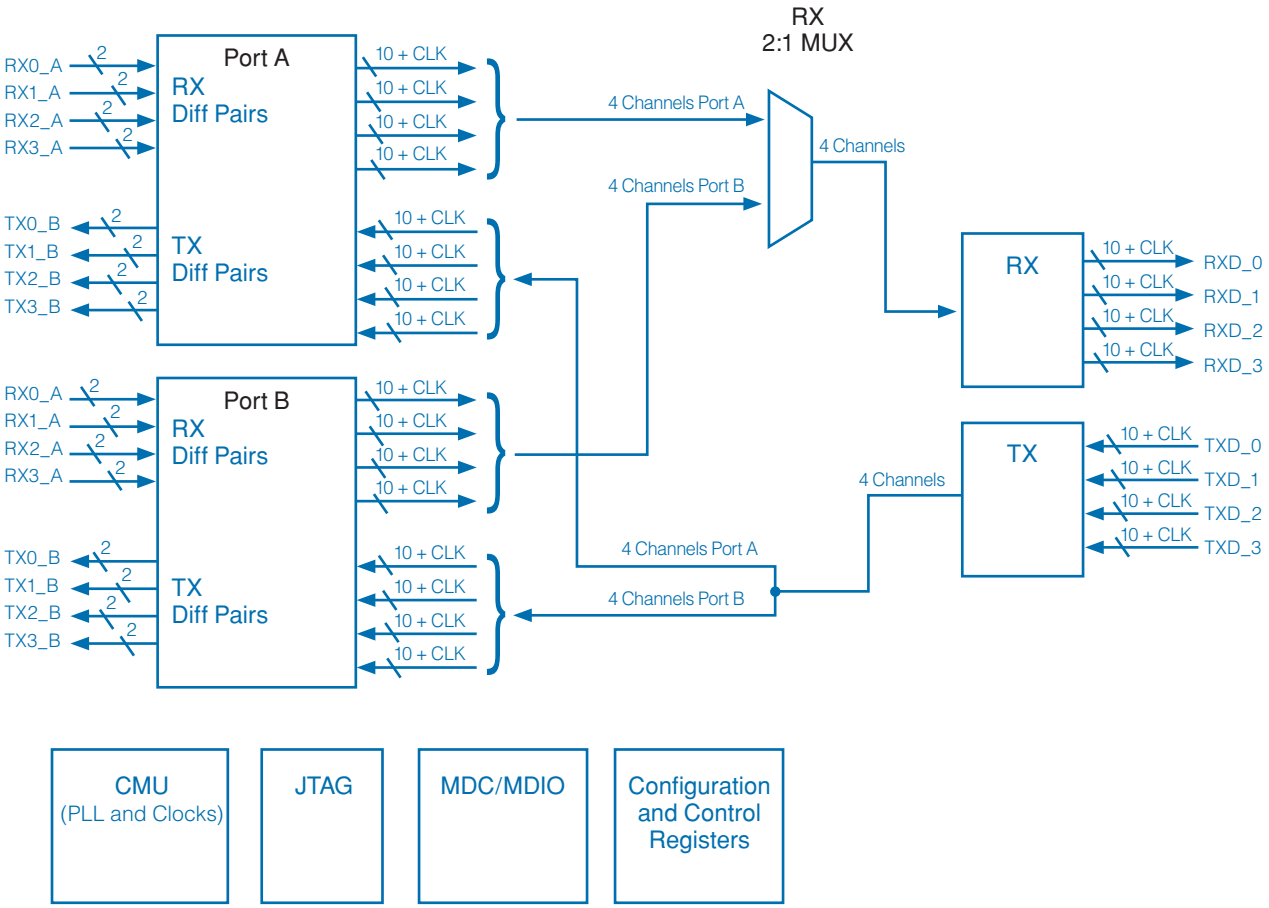
- Supports absolute REFCLK frequency deviation within +/- 100 ppm from nominal standard frequency.
- Support +/- 200 ppm differential between line data rate and local data rate.

Applicable Documents

This document is description of the general operation, performance specifications, features, functions, protocol support and electrical performance. See the HXSRD01 Trivor User's Guide for complete detailed operation.

- HXSRD01 Trivor User's Guide – Detailed information regarding features and operation.
- HXSRD01 Register Description – Detailed description of all the registers.
- HXSRD01 Pinout Document – Provides information on the pinout and I/O description.

Functional Diagram



Signal and I/O Type Definitions

Signal Type	I/O Signal Type
PWR/GND	
Discrete Inputs	CMOS, CMOS with Pullup, CMOS with Pulldown, CMOS Schmitt Trigger
Discrete Outputs	CMOS, CMOS Tri-state
Ref Clock Input	LVPECL
Reference Voltage Output	1.25V source
Resistor Bias	15k ohm resistors
MDIO	CMOS Bidirectional
Parallel Tx Data and Clock	SSTL-2
Parallel Rx Data and Clock	SSTL-2
Serial Tx	SERDES 50 ohms
Serial Rx	SERDES 50 ohms

Absolute Maximum Ratings (1)(2)

Symbol	Parameter	Ratings Min	Max	Units
VDD	Supply Voltage (core) (3)(4)	-0.5	2.5	Volts
V_{DD2}	Supply Voltage (I/O) (3)(4)	-0.5	4.6	Volts
V_{PIN}	Voltage on Any Pin (3)(4)	-0.5	VDDx + 0.5	Volts
PD	Package Power Dissipation		2.8	Watts
V_{PROT}	Electrostatic Discharge Protection Voltage (5)	1000		V
T_{STORE}	Storage Temperature	-65	150	°C
T_{SOLDER}	Soldering Temperature (6)		270	°C
T_J	Maximum Junction Temperature		175	°C
P_{JC}	Package Thermal Resistance (Junction to Case) (7)		3.6	°C /W

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to V_{SS}.
(3) VDDx (relevant supply) must be at recommended DC level. When VDDx is above recommended levels then absolute limits for inputs and outputs are capped by the limit for VDDx.
(4) Absolute maximum levels for cold spare I/O when VDDx is 0V are the same as the limit for the relevant VDDx.
(5) Class 1C electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015
(6) Maximum soldering temp of 270°C can be maintained for no more than 5 seconds.
(7) Value provided assumes 2.2 mm columns. Parts are shipped without columns.

Recommended Operating Conditions (1)

Symbol	Parameter	Min	Description Typical	Max	Units
VDD	Supply Voltage (core)	1.71	1.80	1.89	Volts
V_{DD2}	Supply Voltage (I/O)	2.3	2.5	2.7	Volts
V_{PIN} (CMOS)	Voltage on CMOS I/O Pins	-0.3		VDDx + 0.3	
V_{PIN} (LVPECL DC) (2)	DC Voltage on LVPECL Pins	-0.13		VDDx + 0.3	Volts
V_{PIN} (LVPECL Diff) (3)	Differential Voltage on LVPECL Pins	0.10		VDD	Volts
V_{PIN} (LVPECL DC CM) (4)	Common Mode on LVPECL Pins	–		–	Volts
T_C	External Package Temperature	-55	25	125	°C

(1) Voltages referenced to V_{SS}
(2) This specifies the maximum allowable DC delta between the two inputs.
(3) This specifies the minimum input differential voltage required for switching. This differential voltage is VINP-VINN.
(4) These signals must be AC coupled.

Radiation Characteristics

Total Ionizing Radiation Dose

Trivor will meet all stated functional and electrical specifications after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications, post rebound (based on extrapolation), after an operational period of 15 years. Total dose hardness is assured by wafer level testing of process monitor transistors using 10 KeV X-ray. Parameter correlations have been made between 10 KeV X-rays applied at a dose rate of $5x10^5$ rad(SiO_2)/min at T= 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

Trivor is capable of complete operation during and after exposure to a transient ionizing radiation pulse, up to the specified transient dose rate upset level, when applied while operating under recommended operating conditions. It is recommended to provide external power supply decoupling capacitors to maintain VDD voltage levels during transient events. Trivor will meet any functional or electrical specification after exposure to a radiation pulse up to the transient dose rate survivability specification, when applied under recommended operating conditions. Note that the current conducted during the pulse by the Trivor inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

Trivor will meet any functional or timing specification after exposure to the specified neutron fluence, assuming the device has operated consistent with the recommended operating and storage conditions. The specification assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

Trivor will have a soft error rate contribution to the Bit Error Ratio (BER) while operating under the recommended operating conditions. The specification applies to both heavy ions and protons. This heavy ion hardness level is defined by the Adams 90% worst case cosmic ray environment for geosynchronous orbits. Trivor has a non-radiation environment specified BER of $1X10^{-12}$. This specified BER is a result of meeting the IEEE802.3, Clause 39 Total and Deterministic Jitter requirements. The contribution to BER due to single event upsets is negligible compared to the IEEE802.3 BER specification.

Latchup

Trivor will not latch up due to any of the above radiation exposure conditions when applied under the recommended operating conditions. Fabrication with the SOI substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p- and n-channel substrates are made to ensure no source/drain snapback occurs.

Radiation-Hardness Ratings (1)

Parameter		Limits	Units	Test Conditions
Total Dose Level-H Level-F		$\geq 1 \times 10^6$ $\geq 3 \times 10^5$	Rads(Si)	TA = 25°C, VDD2 = 2.7V, VDD = 1.89V
Transient Dose Rate Upset		$\geq 1 \times 10^{10}$	Rads(Si)/s	Pulse width = 50 ns, X-ray, VDD2 = 2.3V, VDD = 1.71V, T_C = 25°C
Transient Dose Rate Survivability		$\geq 1 \times 10^{12}$	Rads(Si)/s	Pulse width = 50 ns, X-ray, VDD2 = 2.7V, VDD = 1.89V, T_A = 25°C
Bit Error Rate (2)	Heavy Ion Proton	$< 1 \times 10^{-12}$ $< 1 \times 10^{-12}$	bit upsets / bits sent	VDD2=2.3V, VDD=1.71V, TC= 25 and 125°C, Adams 90% worst case environment
Neutron Fluence		$\geq 1 \times 10^{14}$	N/cm^2	1 MeV equivalent energy, Unbiased, T_A = 25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.

(2) The Bit Error Ratio (BER) is defined as the number of bit errors per bits sent due to ion-induced single event upsets.

DC Electrical Characteristics (1)

CMOS Inputs and Outputs

Symbol	Parameter	Min	Max	Units	Test Conditions
IIL1	Low Input Leakage CMOS	-407	-116	uA	VDD = 1.89V, Vin = 0V, Pullup mode
		-10	10		VDD = 1.89V, Vin = 0V, Pulldown mode
IIH1	High Input Leakage CMOS	-10	10	uA	VDD = 1.89V, Vin = VDD, Pullup mode
		116	407		VDD = 1.89V, Vin = VDD, Pulldown mode
IOZ1	Output Leakage CMOS	31	186	uA	VDD = 1.71V, Vout = 0.4V
		-186	31		VDD = 1.71V, Vout = 1.31V
VOL1	Low Output Voltage (3mA driver)		0.43	V	IOL = 3mA, VDD = 1.71V, VDDA = 2.3V
VOH1	High Output Voltage (3mA driver)	1.28		V	IOL = -3mA, VDD = 1.71V, VDDA = 2.3V
VOL2	Low Output Voltage (9mA driver)		0.43	V	IOL = 9mA, VDD = 1.71V, VDDA = 2.3V
VOH2	High Output Voltage (9mA driver)	1.28		V	IOL = -9mA, VDD = 1.71V, VDDA = 2.3V
VIL	Low Input Voltage	0.6		V	VDD = 1.71
VIH	High Input Voltage		1.23	V	VDD = 1.89V
Cpin (2)	Pin Capacitance		9		pF

(1) Worst case operating conditions: V_{DD2}=2.3V to 2.7V, V_{DD}=1.71V to 1.89V, -55°C to +125°C. Post-radiation performance guaranteed at 25°C per MIL-STD-883 method 1019 up to 1MRad(Si) total dose.
(2) Guaranteed but not tested.

SSTL-2 Buffer DC Scecifications

Symbol	Description	Min	Typ	Max	Units
VDD2 (1)	Driver supply voltage	2.3	2.5	2.7	V
VOTR	Output timing reference level		0.5 * VDD2		V
Topwr (3)	Power up from/to tri-state delay			3.5	ns
Cpin (3)	Pin capacitance		10		pF

(1) VDD driver and VDD receiver need to be connected to the same supply and must track each other.
(2) Not applicable.
(3) Guaranteed by design.

SSTL-2 Inputs and Outputs

Symbol	Parameter	Min	Max	Units	Test Conditions
IIL	Low Input Leakage SSTL	-10	10	uA	Vin = 0V, VDD = 1.89V, VDDA = 2.7V
IIH	High Input Leakage SSTL	-10	10	uA	Vin = VDD2, VDD = 1.89V, VDDA = 2.7V
IIH REF	Output Leakage SSTL REF	-10	10	uA	VIN = VDD/2, VDD = 1.89V, VDDA = 2.7V
IOZL	Output Leakage Current	-680	-170	uA	Vout = 0V, , VDD = 1.89V, VDDA = 2.7V
IOZH	Output Leakage Current`	170	680	uA	Vout = 0V, , VDD = 1.89V, VDDA = 2.7V
VOH (AC)	High Output Voltage	VTT + 0.608		V	(1)
VOL (AC)	Low Output Voltage		VTT - 0.608	V	(1)
VIH (DC)	DC High Input Voltage	VREF + 0.15	VDD2 + 0.3	V	(1)
VIL (DC)	DC Low Input Voltage	-0.3	VREF - 0.15	V	(1)
VIH (AC)	AC High Input Voltage	VREF + 0.31	1.38	V	(1)
VIL (AC)	AC Low Input Voltage		VREF – 0.31	V	(1)
VOL	Low Output Voltage		0.76	V	VDD = 1.71
VOH	High Output Voltage	1.54		V	VDD = 1.89V
Fdata	Data Rate		250	MHz	
VREF IN	Input Reference Voltage	1.13	1.38	V	Typical VREF IN = 1.25V
VREF OUT	Output Reference Voltage	1.035	1.265	V	Io = 0mA, VDD = 1.71, VDD2 = 2.3V
		1.215	1.481		Io = 0mA, VDD = 1.89, VDD2 = 2.7V
VTT	Termination Voltage	VREF – 0.04	VREF + 0.04		

(1) Guaranteed but not tested.

LVPECL Inputs

Symbol	Description	Min	Typ	Max	Units
IIL	Input Leakage Low (3)	-10		10	uA
IIH	Input Leakage High (4)	-10		10	uA
VIN (DC)	DC input signal voltage	-0.13		VDD + 0.3	V
VDIF (DC)	DC differential input voltage (1)	0.1		VDD	V
VCM (DC)	DC common mode voltage (2)	VSS + 0.4	VDD / 2	VDD – 0.4	V
VDIF (AC)	AC differential input voltage (1)	0.2		1.5	V
Cin	Input pin capacitance (5)		11		pF
PLL Lock Time	Maximum time for the PLL to achieve lock after power and REFCLK clock are present (5)			40	ms
REFCLK Jitter	Maximum wideband REFCLK peak-to-peak jitter			50	ps
REFCLK Jitter	Narrowband REFCLK peak jitter (12 kHz to 20 MHz)			20	ps
REFCLK Rise/Fall Time	REFCLK rise/fall time (10% - 90%).			800	ps

(1) Measured in differential peak-to-peak voltage. Spec is only for test purposes.
(2) Designed for an AC-coupled interface between the buffer and the external oscillator.
(3) Test Conditions: VDD = 1.89, VIN = 0V
(4) Test Conditions: VDD = 1.89, VIN = 1.89V
(5) Guaranteed but not tested.

LVPECL Inputs

Symbol	Description	Min	Typ	Max	Units
V_{INDIFF} (1)	Differential Input Amplitude	150		VDDA + 0.3	mV p-p
IIH, IIL	Input leakage current	-20		20	µA
V_{INCM} (2)	Differential Input Common Mode		NA		mV
RX_TJ (3) (4)	RX total Jitter Tolerance at the high-speed receiver. 1GE			0.68	UI
	RX total Jitter Tolerance at the high-speed receiver. 10GE			0.65	UI
	RX total Jitter Tolerance at the high-speed receiver. 1GFC			0.68	UI
	RX total Jitter Tolerance at the high-speed receiver. 2GFC			0.62	UI
	RX total Jitter Tolerance at the high-speed receiver. 10GFC			0.65	UI
RX_DJ (3)	RX deterministic jitter tolerance at the high-speed receiver. 1GE			0.33	UI
	RX deterministic jitter tolerance at the high-speed receiver. 10GE			0.37	UI
	RX deterministic jitter tolerance at the high-speed receiver. 1GFC			0.33	UI
	RX deterministic jitter tolerance at the high-speed receiver. 2GFC			0.37	UI
	RX deterministic jitter tolerance at the high-speed receiver. 10GFC			0.37	UI
$V_{OUTDIFF}$ (1)	Differential Output Amplitude	600	1200	1600	mVp-p
V_{OUTCM} (1) (3)	Differential Output Common Mode	0.8	VDDA / 2	1	V
Tr, Tf (3)	Differential Output Rise and Fall Time (20% - 80%)		90		ps
TX_TJ (3)	Total Jitter on the high-speed transmit output buffer. 1GE			0.23	UI
	Total Jitter on the high-speed transmit output buffer. 10GE			0.35	UI
	Total Jitter on the high-speed transmit output buffer. 1GFC			0.23	UI
	Total Jitter on the high-speed transmit output buffer. 2GFC			0.33	UI
	Total Jitter on the high-speed transmit output buffer. 10GFC			0.35	UI
TX_DJ (3)	Deterministic Jitter on the high-speed transmit output buffer. 1GE			0.11	UI
	Deterministic Jitter on the high-speed transmit output buffer. 10GE			0.17	UI
	Deterministic Jitter on the high-speed transmit output buffer. 1GFC			0.11	UI
	Deterministic Jitter on the high-speed transmit output buffer. 2GFC			0.2	UI
	Deterministic Jitter on the high-speed transmit output buffer. 10GFC			0.17	UI
Cpin	Pin capacitance		5		pF

(1) Differential peak-to-peak. Pre-emphasis is disabled. Nominal
(2) Designed for an AC-coupled interface
(3) Guaranteed by design; not tested on each part.
(4) Includes 0.10 UI of sinusoidal jitter

Power Supply Current Characteristics

These numbers are nominal values provided for estimating power requirements. They are not tested as part of the electrical screening tests.

Symbol	Parameter	Min	Max	Units	Test Conditions
IDD	VDD Operational Supply Current (1) (2)		2.2	A	
IDD2	VDD2 Operational Supply Current (2) (3)		600	mA	
IDDL	IDD Shutdown Current		16	mA	
IDD2L	IDD2 Shutdown Current		5	mA	

(1) IDD represents the current consumed from the 1.8 V supply. This data represents a 1.89 V and -55°C environment. The current from VDD2 is not included in this specification.
(2) IDD2 represents the current consumed from the 2.5 V supply. This data represents a 2.7 V and -55°C environment. The current from VDD is not included in this specification.
(3) This assumes a configuration for maximum power consumption.

Typical Power Consumption (1) (2) (3) (4) (13)

These numbers are nominal values provided for estimating power requirements. They are not tested as part of the electrical screening tests.

Trivor Configuration	1.0625 Gb/s	2.125 Gb/s	3.125 Gb/s	3.1875 Gb/s
CMU Only (5)	221	306	410	425
Single Port (6)	1087	1363	1766	1786
Single Lane (7) (12)	535	675	902	907
Single Transmit Port (8)	484	612	806	810
Single Transmit Lane (9) (12)	383	488	662	664
Single Receive Port (10)	826	1057	1370	1400
Single Receive Lane (11)	373	493	650	668

(1) SSTL-2 power is not included because it consumes power from the 2.5 V supply
(2) SSTL-2 power estimate is 450 mW per port or 112.5 mW per lane
(3) Power numbers are based on transmitting and receiving the CJTPAT
(4) The 1.8 V power consumptions includes the VDD and VDDA supply power which provides power to the analog SERDES macro and Trivor logic.
(5) CMU power includes the PLL and associated clock trees
(6) Full port power includes both transmit and receive channels for 4 lanes and the CMU power
(7) Full lane power includes both transmit and receive channels for 1 lane and the CMU power
(8) Transmit port power includes only the transmit channels for 4 lanes and the CMU power
(9) Transmit lane power includes only the transmit channels for 1 lane and the CMU power
(10) Receive port power includes only the receive channels for 4 lanes and the CMU power
(11) Receive lane power includes only the receive channels for 1 lane and the CMU power
(12) The average power per transmit lane decreases as additional lanes are utilized within a port due to port level clock distribution overhead.
(13) These are typical values and are not tested on a part-by-part basis

Recommended External Components

Description	Value	Comments
REFCLK AC-Coupling Capacitors (CREFCLK) (1)	0.01 µF	Ceramic capacitors are recommended
Serial Input AC Coupling Capacitors (CRXIN) (2)	0.01 µF	Ceramic capacitors are recommended
External Bias Resistor	15 kΩ ± 1%	Resistor is connected between the RREF and REXT pins
Power Supply Filter (3)	100 µF	Distribute the power supply capacitors as close to the part as possible. Honeywell recommends using 0.01 µF and 0.1 µF capacitors close to the chip and larger capacitors farther away. The Trivor evaluation board also uses a series inductor (0.1 µH) in the power supply lines.
Oscillator	100 – 160 MHz	The oscillator selected needs to meet the minimum differential input voltage specification of the LVPECL receiver. The maximum offset in frequency between oscillators sourcing the clock for separate chips communicating together is ±100 ppm

(1) If REFCLK is being driven with a single-ended oscillator the AC-coupling capacitor does not need to be connected to the inverting terminal (REFCLKN). REFCLKN should float in this case.
(2) CRXIN should be placed as close as possible to the part. Routes between the CRXIN capacitors and the part need to be matched in impedance and length.
(3) VDD and VDDA domains should be connected at the board level.

Two Wire Serial Interface

The Quad redundant SERDES includes a two wire serial management interface for register access. The interface supports MDC/MDIO interface per clause 45 of IEEE 802.3ae. The MDC/MDIO interface supports access at 2.5 MHz with indirect addressing per the IEEE specifications as well as 25 MHz faster mode.

MDCMIO per 10GE IEEE Standard 802.3ae

	Management Frame Fields							
Frame	PRE	ST	OP	PRTAD	DEVAD	TA	Adress / Data	Idle
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

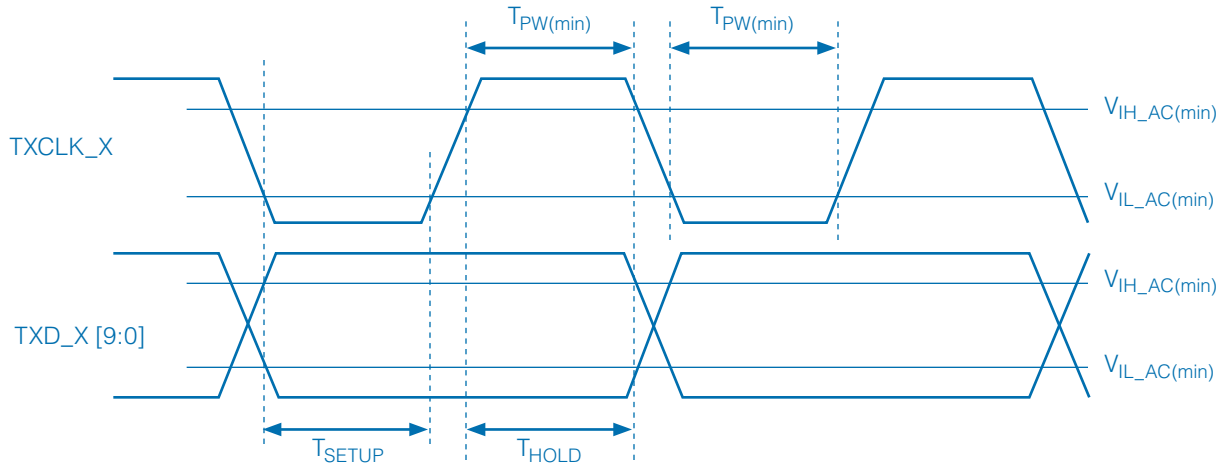
Parallel Port Timing – SSTL Interface

In the transmit path, there is a setup and hold relationship between the clock and data input signals described in the Transmit Timing Parameters table. The transmit path is referenced to the direction of the serial data stream. Therefore, the transmit interface is actually timing at the parallel port receive buffers. The figures below illustrate SDR and DDR modes. The clock for the incoming parallel data must be the same as the REFCLK into the CMU (0 ppm).

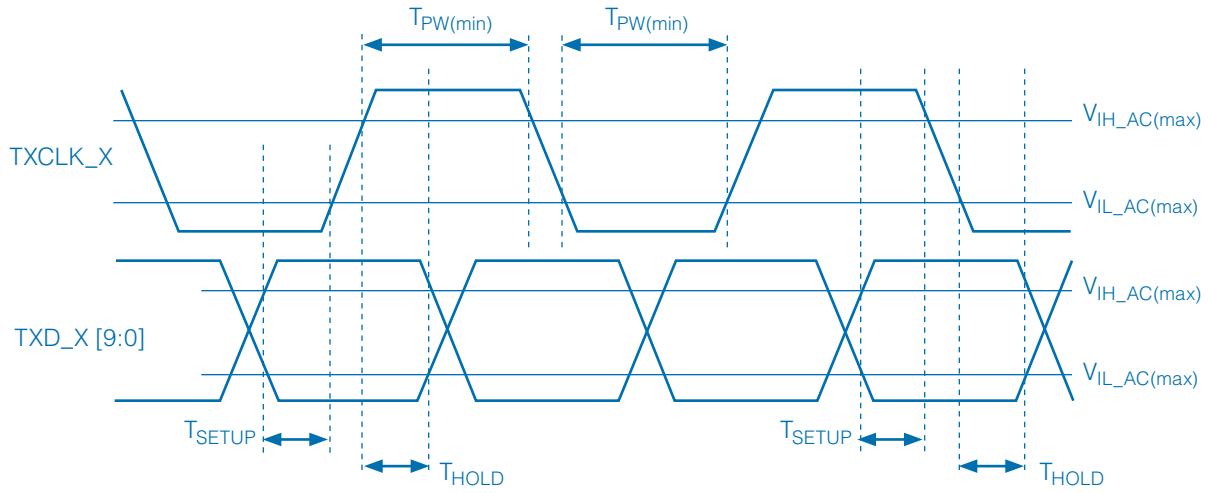
Symbol	TXCLK/TXDATA	Units
t_{setup}	-810	ps
t_{hold}	1620	ps
T_{pwmin}	2.5	ns

(1) The TXCLK and TXDATA relationship are for the SSTL receive buffers on the parallel receive side. The “RX” nomenclature is in relation to the serial interface.

Transmit SDR Timing Diagram for Parallel Interface



Transmit DDR Timing Diagram for Parallel Interface



Receive Parallel Interface

In the receive path, there is a timing relationship between the clock and data output signals described in the Receive Clock Timing Parameters table below. This timing relationship between the clock and data is best described as a “data valid” window around the clock signals.

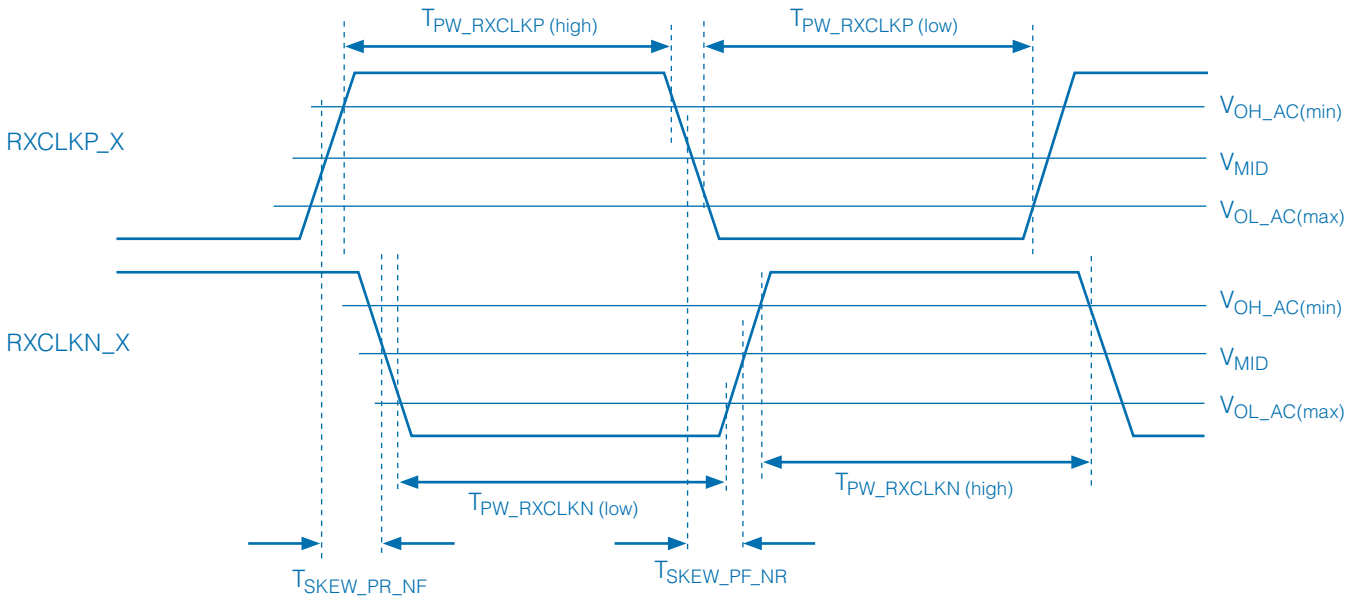
The parallel receive side offers both a true and complement clock for each of the 4 lanes, RXCLKP_<lane> and RXCLKN_<lane>, respectively. The receive data is internally clocked on the RXCLKP_<lane> for each lane independently. RXCLKN_<lane> is generated by a logical inversion of RCLKP_<lane>. Receive timing can key off either the true or the complement. The diagram below shows the relationship between RXCLKP_<lane> and RXCLKN_<lane>.

Receive Clock Timing Parameters

Symbol	Lane 0	Lane 1	Lane 2	Lane 3	Units
$T_{pw\ rxclkp(high)}$ **MIN**	3070	2910	2880	3330	ps
$T_{pw\ rxclkp(low)}$ **MIN**	3130	3160	3170	2880	ps
$T_{pw\ rxclkn(low)}$ **MIN**	3150	2990	2960	3340	ps
$T_{pw\ rxclkn(high)}$ **MIN**	3070	3110	3130	2860	ps
$T_{skew\ pr\ nf}$ **MAX**	130	130	150	180	ps
$T_{skew\ pf\ nr}$ **MAX**	210	200	230	200	ps

(1) The pulse widths shown are measured with the fastest supported speed or Trivor representing a worst case. Pulse width will increase as speed decreases.

RXCLKP to RXCLKN Timing Diagram



The receive path is referenced to the direction of the serial data stream. Therefore, the receive interface is actually timing at the parallel port transmit buffers. The timing parameters between the receive clock and data are described as setup and hold times. The figures below illustrate SDR and DDR modes and are referenced to RXCLKP_<lane>.

The data is SDR or DDR depending on mode of operation; rate of operation as explained below.

This data is related to the RXCLKN<lane> and RXCLKP<lane> clocks.

Rate, Mode	DDR/SDR
2.125 Gbps FC	DDR
1.0625 Gbps FC	DDR
3.125 Gbps 10GE	DDR
3.1875 Gbps 10GFC	DDR
1.25 Gbps GE	SDR

This data is related to the TXCLK<lane> clock.

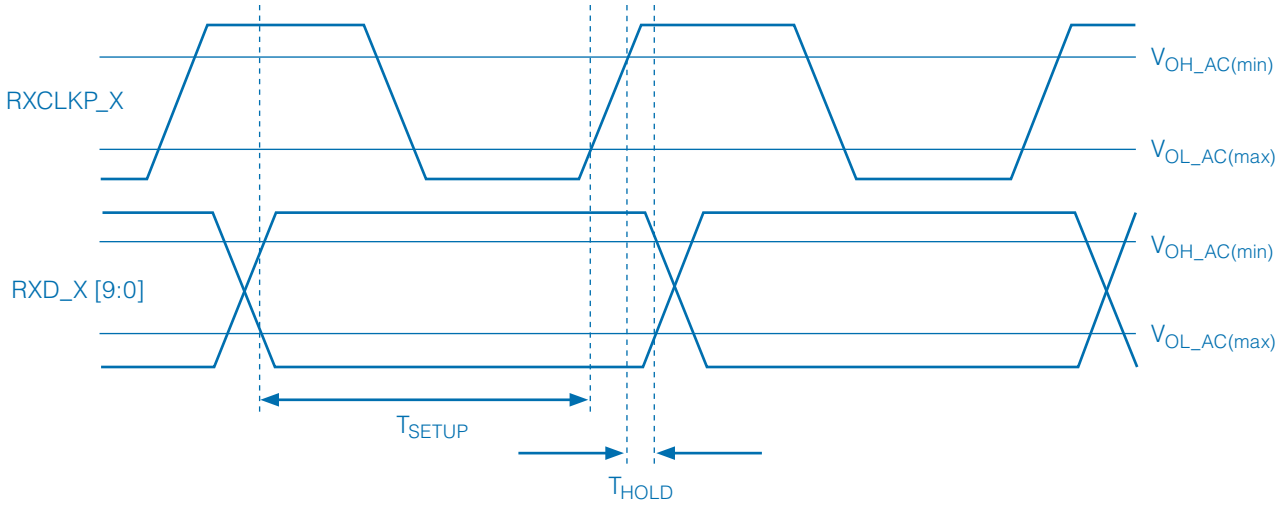
Rate, Mode	DDR/SDR
2.125 Gbps FC	DDR
1.0625 Gbps FC	SDR
3.125 Gbps 10GE	DDR
3.1875 Gbps 10GFC	DDR
1.25 Gbps GE	SDR

Receive Timing Parameters

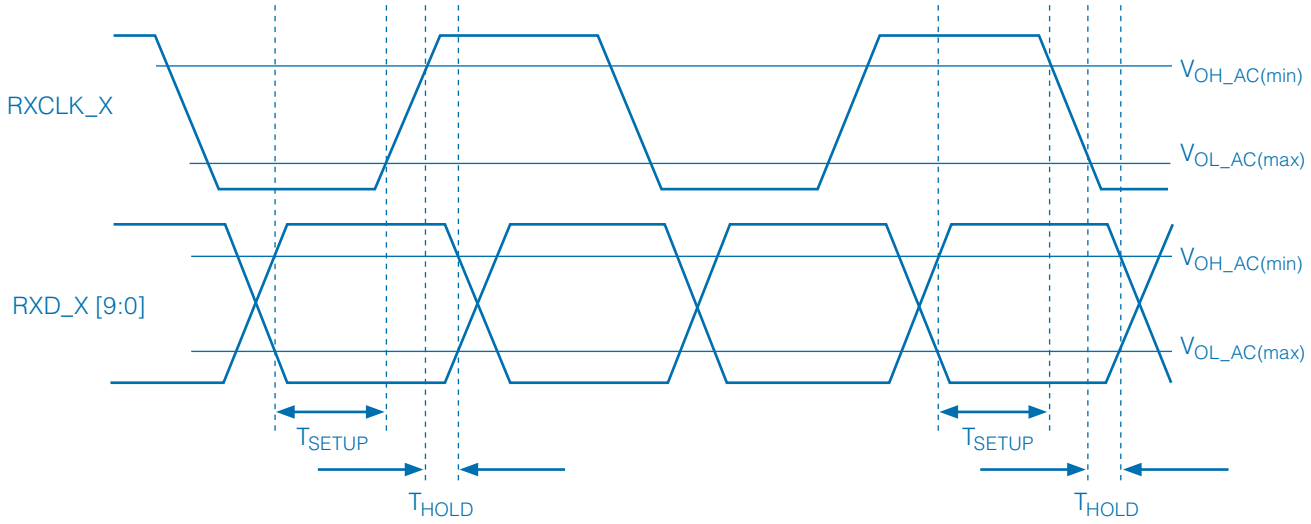
Symbol	Lane 0	Lane 1	Lane 2	Lane 3	Units
$T_{pw\ rxclkp(high)}$ **MIN**	3070	2910	2880	3330	ps
$T_{pw\ rxclkp(low)}$ **MIN**	3130	3160	3170	2880	ps
$T_{pw\ rxclkn(low)}$ **MIN**	3150	2990	2960	3340	ps
$T_{pw\ rxclkn(high)}$ **MIN**	3070	3110	3130	2860	ps
$T_{skew\ pr\ nf}$ **MAX**	130	130	150	180	ps
$T_{skew\ pf\ nr}$ **MAX**	210	200	230	200	ps

(1) The pulse widths shown are measured with the fastest supported speed or Trivor representing a worst case. Pulse width will increase as speed decreases.

Receive SDR Timing Diagram for Parallel Interface

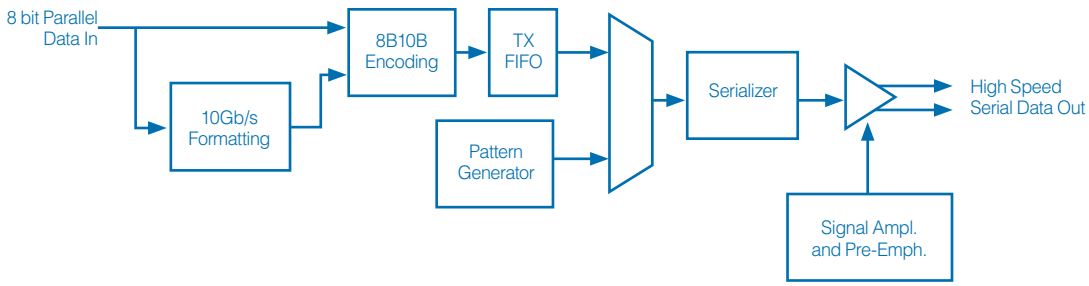


Receive DDR Timing Diagram for Parallel Interface



Functional Electrical Operation

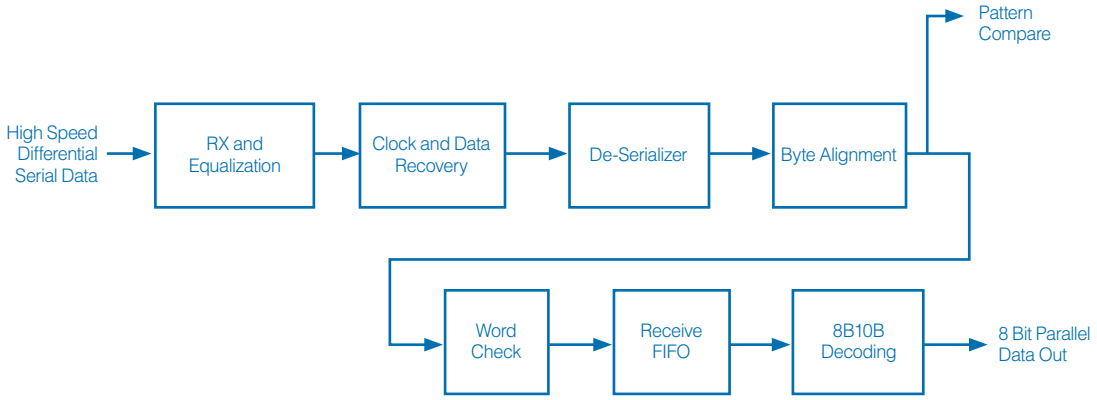
Transmitter



The high speed serial interface has a total of 8 lanes. The data rates for each lane range from 1.0625 Gbps to 3.1875 Gbps. Port A and Port B both include 4 lanes of SERDES transmitter and receiver pairs. Each function will be described as an individual lane and will apply to all lanes. For 10Gbps applications, the data for the 4 lanes is grouped in the Trivor. Each lane can be controlled independently including on/off control, data rate, signal levels, pre-emphasis, and equalization.

The clock for the data coming into the Trivor must be the same as the REFCLK going into the CMU (0 ppm difference). There is no clock compensation on the transmit path. Each transmit lane receives data from an 8 bit parallel bus through SSTL-2 input buffers. Each lane is 8b10b encoded, serialized and transmitted. A transmit FIFO is used to separate the clock domains of the incoming transmit data from the serializer clock domain and control the amount of lane-to-lane skew to within ±100ps. If configured for a XAUI mode, then the four individual lanes are aligned inside the transmit FIFO. Transmitter redundancy is provided in the form of two sets of SERDES ports (A & B). The transmit buffer includes internal 100 Ω differential termination resistance, and is designed to drive an AC coupled channel.

Receiver



Each receive lane receives data through a high speed differential serial receiver. The CDR will recover a clock from the incoming 8b10b encoded data stream.The high speed serial data will then be de-serialized into a 10 bit word, byte aligned, 8b10b decoded and sent out on SSTL-2 transmit buffers. When in XAUI modes, the data from 4 lanes is trunked together to form one 40 bit word. A receive FIFO is used to transfer from the recovered clock domain to the system clock domain. Receiver redundancy is provided in the form of two sets of SERDES ports (A & B). While all 8 receive lanes can be active at once, only one port can send data to the SSTL-2 parallel interface at one time. The receive buffer includes internal 100 Ω differential termination resistance, and is designed to be driven from an AC coupled channel.

Parallel Interface

The parallel interface at the output of each receive lane will provide a complementary clock and 8 bits of data as well as a comma detect and an error detect signal. The data format on the 8 bit interface will depend on the selected protocol and whether or not the 8b10b decoder is enabled. If the decoder is disabled, an un-encoded 10 bit word will be used.

The parallel interface at the input of each transmit lane will receive a single clock and 8 bits of data to be encoded and serialized. If the encoder is disabled, 10 bits of 8b10b encoded data must be provided. The parallel interface operates in a Dual Data Rate (DDR) mode for all protocol configurations with the exception of 1G Ethernet which is Single Data Rate (SDR). This can be configured by the use of internal registers. The parallel interface is implemented using 2.5V SSTL-2 buffers.

Protocols

Trivor was designed to support multiple protocols including Gigabit Ethernet, 10 Gigabit Ethernet XAUI, Fibre Channel and 10 Gigabit Fibre Channel XAUI. The sections below describe what layers of each protocol are supported. Each protocol has a specified packet format that includes a header, body and footer. Device operation requires that these formats be followed for accurate data transmission and recovery.

Gigabit Ethernet

In relation to the Gigabit Ethernet standard, Trivor implements the Physical Medium Attachment (PMA) sublayer and portions of the Physical Coding Sublayer (PCS) in accordance with IEEE802.3-2005 clause 36. Within the PCS, Trivor implements Synchronization and portions of the Transmit and Receive processes. Trivor does not implement Carrier Sense or Auto-Negotiation. Of the PCS Receive functions, Trivor performs decoding and code-group monitoring. The validity of the received code-groups is checked against running disparity rules. Of the PCS Transmit functions, Trivor performs encoding. The transmitted code-groups are generated according to running disparity rules.

10 Gigabit Ethernet XAUI

In relation to the 10 Gigabit Ethernet XAUI standard, Trivor implements the Physical Medium Attachment (PMA) sublayer and portions of the Physical Coding Sublayer (PCS) in accordance with IEEE802.3ae-2002 clause 48. Within the PCS, Trivor implements the Transmit, Synchronization, Deskew, and portions of the Receive processes. Of the PCS Receive functions, Trivor performs decoding and code-group monitoring. The validity of the receive code-groups is checked against running disparity rules.

Fibre Channel

In relation to the Fibre Channel standard, Trivor implements the physical interface (FC-0) and transmission protocol (FC-1) functions. The Trivor physical interface supports electrical transmission media, transmitters, receivers and their interfaces (FC-PI-2 clauses 9 and 10). The Trivor transmission protocol supports serial encoding (clause 5) and decoding (clause 6) from the framing and signaling interface (FC-FS).

Clock Multiplier Unit (CMU)

The single Clock Multiplier Unit (CMU) generates high frequency clock s by multiplying up the reference clock. The multiplication factor can be set to 10, 15, or 20. As a result, each of the 8 lanes of the Trivor must run at either full, half or quarter rate of this base frequency. The CMU also generates the clocks used throughout the chip. When using the device in an application requiring only one to four lanes, Port B should be used and Port A should be powered down because the system clock is derived from Port B.

The REFCLK going into the CMU must be the same as the clock for the parallel port transmit data coming into the Trivor (0 ppm difference). There is no clock compensation on the transmit path.

REFCLK Implementation

The REFCLK input for this device is an LVPECL receiver. The maximum single-ended peak-to-peak input swing per FC-PI-2 Annex B is around VDD/2 or 900 mV. These signals must be AC-coupled externally using 0.01 µF capacitors. These signals will be internally terminated using two 100k Ω terminating resistors connected between VDD and VSS to a VCM point that will act as an AC ground. The internal node will be biased somewhere appropriate between VDD/2 to VDD.

Register Configuration Management Interface

For internal register access, Trivor includes a MDC/MDIO serial management interface per clause 45 of IEEE 802.3ae. The MDC/MDIO interface supports access up to 25 MHz with indirect addressing per the IEEE specifications.

Bandgap and Bias

The bandgap and bias circuitry is used to set the master bias currents used by the high speed logic blocks. A 15 KΩ +/- 1% resistor is to be provided externally for proper biasing.

Serial Loopback

Serial loopback provides a path from the serializer to the clock and data recovery unit. The transmit buffer will continue to transmit data from the serializer while in serial loopback mode. When in serial loopback mode, the data from the receive buffer is ignored. This path is differential and can be used at data rates up to 3.1875 Gbps. Serial loopback can be enabled for each lane with the pin SERCDRENLOOP. To achieve lane synchronization when the device is configured in Serial Loopback Mode, the receivers need to be driven with a valid pattern because byte alignment is dependent on a valid signal being present on the receiver inputs.

Metallic Loopback

Metallic loopback provides a path from the differential receive buffer to the differential transmit buffer. This path is single ended and is intended for data rates below 2 Gbps (1 GHz). Pre-emphasis is not available to a transmit buffer in metallic loopback mode. If a lane is in metallic loopback mode, the serializer for that lane is forced into a reset state and the data from the serializer is ignored by the transmit buffer. Metallic loopback is enabled by the pin METENLOOP.

Integrated Pattern Generators

The HXSRD01 has 15 built in test patterns and pattern comparators. These include both Ethernet, Fibre Channel and XAUI patterns.

Pattern	Description
FC_LOW_FREQ	Fibre Channel Low Frequency Pattern
FC_HR_QR	Fibre Channel Half-rate and quarter-rate square patterns
FC_TEN3_FREQ	Fibre Channel Ten contiguous runs of 3
FC_CRPAT	Fibre Channel-Compliant random data pattern
FC_CJTPAT	Fibre Channel-Compliant TX jitter test bit sequence
FC_CSPAT	Fibre Channel Supply noise test bit sequences
TENGE_HIGH_FREQ	10G Ethernet High Frequency Test pattern Per IEEE Std. 802.3ae-2002 - Annex 48A
TENGE_LOW_FREQ	10G Ethernet Low Frequency Test Pattern Per IEEE Std. 802.3ae-2002 - Annex 48A
TENGE_MX_FREQ	10G Ethernet Mixed-frequency test pattern Test Pattern Per IEEE Std. 802.3ae-2002 - Annex 48A
FC_PRBS	If prbs31sel is false, PRBS7 is selected, else, PRBS31 is selected.
TENGE_CJTPAT	10G Ethernet Continuous jitter test pattern
TENGFC_HIGH_FREQ	10G Fibre Channel High Frequency Pattern, Per Project 1413-D, 10 Gigabit Fibre Channel, Rev 3.5, April 9, 2003 Annex E: XAUI and 8B/10B PCS test patterns
TENGFC_LOW_FREQ	10G Fibre Channel Low Frequency Pattern Per Project 1413-D, 10 Gigabit Fibre Channel, Rev 3.5, April 9, 2003 Annex E: XAUI and 8B/10B PCS test patterns
TENGFC_MX_FREQ	10G Fibre Channel Mixed Frequency Pattern Per Project 1413-D, 10 Gigabit Fibre Channel, Rev 3.5, April 9, 2003, Annex E: XAUI and 8B/10B PCS test patterns
TENGFC_CJTPAT	10G Fibre Channel-Compliant transmit jitter test bit sequence

Registers

The Trivor has registers are designed to be accessible via a MDC/MDIO interface. The purpose of these registers is to both configure and control the Trivor as well as to indicate status during operation.

Several functions can be controlled by either signal I/O pins or via the configuration registers. The default mode is pin control. There is a pin override register bit that needs to be asserted for the register setting to take control. Detail description of all the registers can be found in the HXSRD01 Register Description document.

Register Functions

- 10GE XAUI Control and Status
- Transmit and Receive Lane Control and Status
- Transmit waveform control
- Receiver Configuration and Equalization
- CMU and Clock Control
- Pattern Generator and Comparator Control
- Configuration control by pin or register (Pin Override)

Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990.

Using this proven approach Honeywell will assure the reliability of the products manufactured with the S150 process technology. This approach includes adhering to Honeywell's General Manufacturing Standards for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, negative bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- A statistically controlled wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- The use of characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

Qualification and Screening

The S150 technology was qualified by Honeywell after meeting the criteria of the General Manufacturing Standards and is QML Qualified. This approval is the culmination of years of development and requires a considerable amount of testing, documentation, and review.

The test flow includes screening units with the defined flow (Class V and Q+) and the appropriate periodic or lot conformance testing (Groups B, C, D, and E). Both the S150 process and the Trivor product are subject to period or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests, respectively.

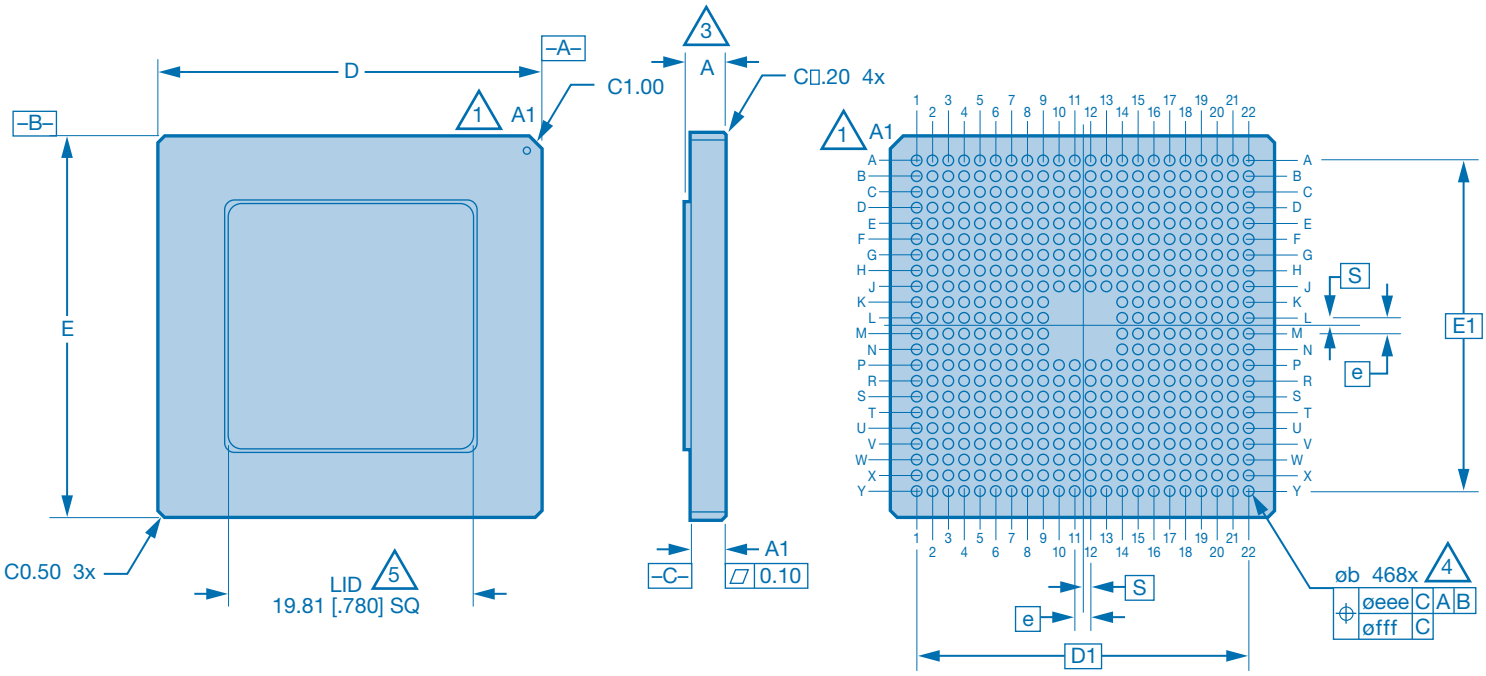
Group A	General Electrical Tests
Group B	Mechanical – Dimensions, Bond Strength, Solvents, Die Shear, Solderability, Lead Integrity, Seal, Acceleration
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package related mechanical tests – Shock, Vibration, Accel, Salt, Seal, Lead Finish Adhesion, Lid Torque, Thermal Shock, Moisture Resistance
Group E	Radiation Tests

Honeywell delivers products that are tested to meet your requirements. Products can be screened to several levels including Engineering Models, and Flight Units. EMs are available with limited screening for prototype development and evaluation testing.

Packaging

The package is 468-lead ceramic LGA. Pin A1 is in the upper right hand corner of the package when the columns are facing down. Rows 10-13 in columns K-N are unpopulated. Solder columns are the recommended method of attaching these components to a circuit board.

Packaging Outline



5. Lid centered on package.
4. b = diameter of the metalized LGA pad.
3. Distance from bottom of the ceramic to the top of the lid.
2. Controlling dimensions are in millimeters.
1. The A1 corner is identified by a larger chamfer and a dot on the top ceramic surface.

Dim	Millimeters Min	Nom	Max	Inches Min	Nom	Max
A	–	3.12	3.43	–	.123	.135
A1	2.42	2.69	2.96	.095	.106	.117
b	0.81	0.86	0.91	.032	.034	.036
DE	30.80	31.00	31.20	1.213	1.220	1.228
D1 E1		26.67			1.050	
e		1.27			0.050	
S		0.635			0.025	
eee		0.30			0.012	
fff		0.15			0.006	

Pinout Listing

Pin	Signal Name
A1	VSSA
A2	VDDA
A3	RXN1 B
A4	VDDA
A5	RXP2 B
A6	VDDA
A7	RXP3 B
A8	VDD2
A9	RXCLKN 3
A10	RXD3[6]
A11	RXD2[1]
A12	RXD2[5]
A13	VSS
A14	COMDET 2
A15	RXD1[3]
A16	RXCLKN 1
A17	RXD1[9]
A18	VDD2
A19	RXD0[5]
A20	RXCLKN 0
A21	COMDET 0
A22	RXALOSLVL 1
B1	RXP0 B
B2	RXN0 B
B3	RXP1 B
B4	VSSA
B5	RXN2 B
B6	VSSA
B7	RXN3 B
B8	RXD3[0]
B9	RXCLKP 3
B10	RXD3[7]
B11	VDD2
B12	RXD2[4]
B13	RXCLKN 2
B14	RXERR 2
B15	RXD1[2]
B16	VSS
B17	RXD1[8]
B18	RXERR 1
B19	RXD0[4]
B20	RXCLKP 0
B21	VDD2
B22	VSS
C1	VDDA
C2	VSSA
C3	VDDA
C4	VDDA
C5	VSSA
C6	VDDA
C7	VSSA
C8	RXD3[1]
C9	VSS
C10	RXD3[8]
C11	RXD2[0]
C12	RXD2[3]
C13	RXCLKP 2
C14	VDD2
C15	RXD1[1]
C16	RXCLKP 1
C17	RXD1[7]
C18	COMDET 1
C19	VSS
C20	RXD0[6]
C21	RXERR 0
C22	ANODE
D1	TXP3 B
D2	TXN3 B
D3	VSSA
D4	ENPATTERNGEN 0
D5	ENPATTERNGEN 1
D6	ENPATTERNGEN 2
D7	VDD
D8	RXD3[2]
D9	RXD3[5]
D10	RXD3[9]
D11	RXERR 3
D12	VSS
D13	RXD2[6]
D14	RXD2[9]
D15	RXD1[0]
D16	RXD1[5]
D17	VDD2
D18	RXD0[0]
D19	RXD0[3]
D20	RXD0[7]
D21	RXD0[9]
D22	CATHODE
E1	VDDA
E2	VSSA
E3	VDDA
E4	ENPATTERNGEN 3
E5	VSS
E6	TRSTB
E7	TDO
E8	RXD3[3]
E9	RXD3[4]
E10	VDD2
E11	COMDET 3
E12	RXD2[2]
E13	RXD2[7]
E14	RXD2[8]
E15	VSS
E16	RXD1[4]
E17	RXD1[6]
E18	RXD0[1]
E19	RXD0[2]
E20	VDD2
E21	RXD0[8]
E22	LANESWAP
F1	TXP2 B
F2	TXN2 B
F3	TDI
F4	TCK
F5	TMS
F6	DVADDR[0]
F7	DVADDR[1]
F8	VSS
F9	VDD2
F10	VSS
F11	VDD2
F12	VSS
F13	VDD2
F14	VSS
F15	VDD2
F16	VSS
F17	VDD2
F18	VSS
F19	CDRTGCNTO[3]
F20	CDRTGCNTO[2]
F21	CDRTGCNTO[1]
F22	CDRTGCNTO[0]
G1	VDDA
G2	VSSA
G3	DVADDR[2]
G4	DVADDR[3]
G5	DVADDR[4]
G6	TSTCLK
G7	VSS
G8	VDD
G9	VSS
G10	VDD
G11	VSS
G12	VDD
G13	VSS
G14	VDD
G15	VSS
G16	VDD
G17	BGAPBYPASS
G18	VDD2
G19	RXDDEBUG[0]
G20	CDRTGCNTOCK
G21	VSS
G22	CDRTGCNTO[4]
H1	TXP1 B
H2	TXN1 B
H3	SCANTST
H4	VSS
H5	CDRPR[0]
H6	CDRPR[1]
H7	VDD
H8	VSS
H9	VDD
H10	VSS
H11	VDD
H12	VSS
H13	VDD
H14	VSS
H15	VDD
H16	VSS
H17	IDDQ
H18	VSS
H19	VDD2
H20	RXDDEBUG[3]
H21	RXDDEBUG[2]
H22	RXDDEBUG[1]
J1	VDDA
J2	VSSA
J3	CDRPR[2]
J4	CDRPR[3]
J5	RXALOSLVL[0]
J6	VREFR
J7	VSS
J8	VDD
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	VSS
J14	VSS
J15	VSS
J16	VDD
J17	VSS
J18	VDD2
J19	RXDDEBUG[6]
J20	RXDDEBUG[5]
J21	RXDDEBUG[4]
J22	VDD2
K1	TXP0 B
K2	TXN0 B
K3	VDDA

Pinout Listing

Pin	Signal Name
K4	PLL VSSA
K5	VDD
K6	PLL VDDA
K7	VDD
K8	VSS
K9	VSS
K14	VSS
K15	VDD
K16	VSS
K17	TESTMODE
K18	VSS
K19	RXDDEBUG[9]
K20	VSS
K21	RXDDEBUG[8]
K22	RXDDEBUG[7]
L1	REXT
L2	VSSA
L3	VDDA
L4	RREF
L5	PLL VSSD
L6	REFCLK N
L7	VSS
L8	VDD
L9	VSS
L14	VSS
L15	VSS
L16	VDD
L17	DEBUGSEL[0]
L18	VDD2
L19	VSS
L20	VDD2
L21	VSS
L22	VDD2
M1	VBG EXT
M2	VSSA
M3	ATB P
M4	ATB N
M5	PLL VDDD
M6	REFCLK P
M7	VDD
M8	VSS
M9	VSS
M14	VSS
M15	VDD
M16	VSS
M17	DEBUGSEL[1]
M18	DEBUGSEL[2]
M19	DEBUGSEL[3]
M20	CMUDIV[1]
M21	VDD
M22	REFCLKSESEL
N1	RXN3 A
N2	RXP3 A
N3	VREFT
N4	VDD
N5	RXEQ[2]
N6	RXEQ[1]
N7	VSS
N8	VDD
N9	VSS
N14	VSS
N15	VSS
N16	VDD
N17	BYTEINVERT
N18	BITINVERT
N19	VSS
N20	REGFILERESET

Pin	Signal Name
N21	FIFORESETIN
N22	BYPASSTXPCS
P1	VDDA
P2	VSSA
P3	RXEQ[0]
P4	RXEQON
P5	SERCDRENLOOP
P6	METENLOOP
P7	VDD
P8	VSS
P9	VSS
P10	VSS
P11	VSS
P12	VSS
P13	VSS
P14	VSS
P15	VDD
P16	VSS
P17	VDD
P18	BYPASSDECODE
P19	BYPASSENCODE
P20	RXRATESEL3[0]
P21	RXRATESEL3[1]
P22	VSS
R1	RXP2 A
R2	RXN2 A
R3	LANESEL[0]
R4	LANESEL[1]
R5	VSS
R6	PORTSEL
R7	VSS
R8	VDD
R9	VSS
R10	VDD
R11	VSS
R12	VDD
R13	VSS
R14	VDD
R15	VSS
R16	VDD
R17	TXRATESEL2[0]
R18	RXRATESEL2[1]
R19	RXRATESEL2[0]
R20	VDD
R21	TXRATESEL3[1]
R22	TXRATESEL3[0]
S1	VDDA
S2	VSSA
S3	RESET
S4	MODE[2]
S5	MODE[1]
S6	MODE[0]
S7	VDD
S8	VSS
S9	VDD
S10	VSS
S11	VDD
S12	VSS
S13	VDD
S14	VSS
S15	VDD
S16	VSS
S17	TXRATESEL1[1]
S18	VSS
S19	TXRATESEL1[0]
S20	RXRATESEL1[1]
S21	RXRATESEL1[0]

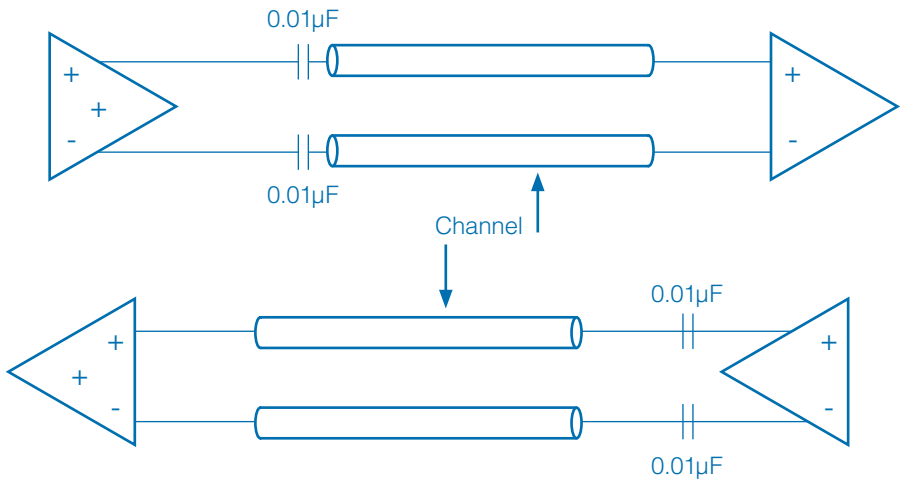
Pin	Signal Name
S22	TXRATESEL2[1]
T1	RXN1 A
T2	RXP1 A
T3	VSSA
T4	MDC
T5	MDIOSEL
T6	RXALOS
T7	TXPE[0]
T8	TXPE[1]
T9	TXPE[2]
T10	CMUDIV[0]
T11	RXACCOUPLED
T12	TXOASEL[2]
T13	TXOASEL[1]
T14	TXOASEL[0]
T15	LANESYNCSTATUS
T16	VDD
T17	PCFRAMESYNC
T18	CRASHDEBUG
T19	TXRATESEL0[1]
T20	TXRATESEL0[0]
T21	RXRATESEL0[1]
T22	RXRATESEL0[0]
U1	VDDA
U2	VSSA
U3	VDDA
U4	VSS
U5	PATTERNSEL[0]
U6	PATTERNSEL[2]
U7	VSS
U8	VDD2
U9	VDD2
U10	VSS
U11	VDD2
U12	VSS
U13	VDD2
U14	VSS
U15	VDD2
U16	VSS
U17	VDD2
U18	VSS
U19	VDD2
U20	VSS
U21	VDD2
U22	PCMISMATCH
V1	RXN0 A
V2	RXP0 A
V3	VSSA
V4	MDIO
V5	PATTERNSEL[1]
V6	PATTERNSEL[3]
V7	VSS
V8	TXD0[9]
V9	TXD0[6]
V10	TXD0[2]
V11	TXD0[0]
V12	VDD2
V13	TXD1[4]
V14	TXD2[9]
V15	TXD2[8]
V16	TXD2[5]
V17	VSS
V18	TXD2[0]
V19	TXD3[7]
V20	TXD3[2]
V21	VDD2
V22	CMULOCKDET

Pinout Listing

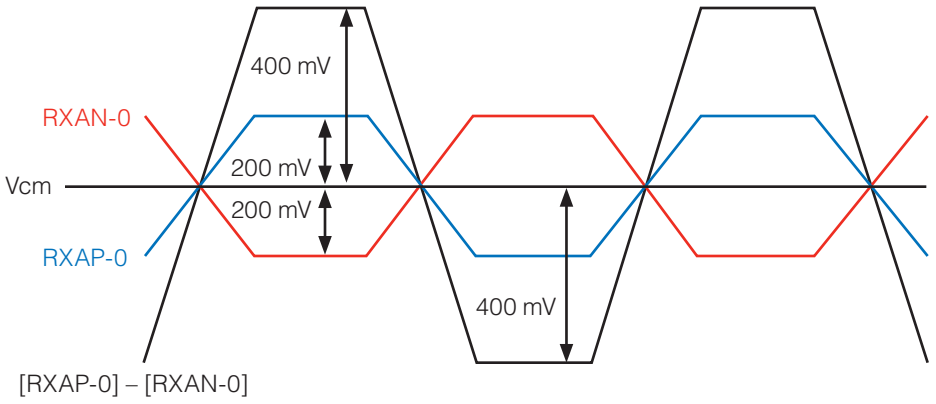
Pin	Signal Name
W1	VDDA
W2	VSSA
W3	VDDA
W4	VSSA
W5	VDDA
W6	VSSA
W7	VDDA
W8	TXD0[8]
W9	TXD0[5]
W10	VSS
W11	TXD1[9]
W12	TXD1[7]
W13	TXD1[3]
W14	TXD1[2]
W15	VDD2
W16	TXD2[4]
W17	TXD2[2]
W18	TXD3[9]
W19	TXD3[6]
W20	VSS
W21	TXD3[1]
W22	VSS
X1	TXN3 A
X2	TXP3 A
X3	TXN2 A
X4	VSSA
X5	TXP1 A
X6	VSSA
X7	TXP0 A
X8	VDD2
X9	TXD0[4]
X10	TXD0[1]
X11	TXD1[8]
X12	TXD1[6]
X13	VSS
X14	TXD1[1]
X15	TXD2[7]
X16	TXD2[3]
X17	TXD2[1]
X18	VDD2
X19	TXD3[5]
X20	TXD3[3]
X21	TXD3[0]
X22	VDD2
Y1	VSSA
Y2	VDDA
Y3	TXP2 A
Y4	VDDA
Y5	TXN1 A
Y6	VDDA
Y7	TXN0 A
Y8	TXD0[7]
Y9	TXD0[3]
Y10	TXCLK0
Y11	VDD2
Y12	TXD1[5]
Y13	TXCLK1
Y14	TXD1[0]
Y15	TXD2[6]
Y16	VSS
Y17	TXCLK2
Y18	TXD3[8]
Y19	TXCLK3
Y20	TXD3[4]
Y21	VDD2
Y22	DSALIGNSTATUS

AC Coupling Guidelines

This device is designed for applications in 100 ohm differential AC-coupled system. The AC coupling capacitors are required as shown in the diagram.



Single-ended and Differential Voltage Levels



RXAP-0, RXAN-0 — Single ended zero to peak voltage = 200 mV; Single ended peak to peak voltage = 400 mV

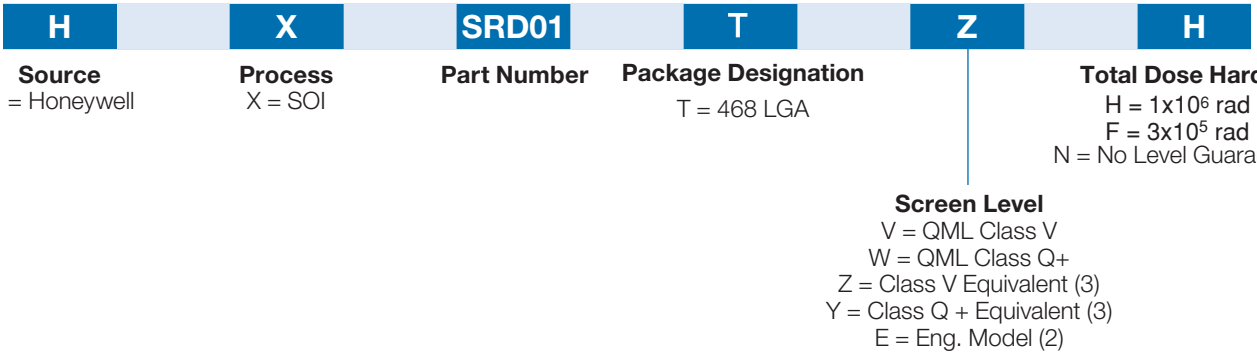
[RXAP-0] – [RXAN-0] — Differential zero to peak voltage = 400 mV; Differential peak to peak voltage = 800 mV

Simulation Models

Simulation models and associated test benches are available upon request. These include:

- Encrypted HSPICE Model: High speed serial interface simulation.
- IBIS Model: Board level signal integrity simulation of other signal I/O excluding the high speed serial interface.
- Verilog Model: Functional simulation of the Trivor
- Verilog Test benches: There are several test benches associated with the Ethernet, Fibre Channel and XAUI configurations.

Ordering Information (1)



(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 for further information.
(2) Engineering Device Description: Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation guaranteed.
(3) These receive the Class V screening. See QCI Testing information below.

QCI Testing (1)

Classification	QCI Testing
QML Q+ and QML Q+ Equivalent	No lot specific testing performed. (2)
QML V and QML V Equivalent	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell Quality Management Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Standard Microcircuit Drawing

The HXSRD01 can be ordered under the SMD drawing 5962-10208.

Find out more

To learn more about Honeywell's family of radiation hardened products and technology, visit www.honeywell.com/radhard.

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