HXLVDSR

Honeywell

Quad LVDS Differential Line Receiver Radiation Hardened 3.3V SOI CMOS

Features

- Four Independent Receivers
- Rad Hard: 300k Rad(Si) Total Dose
- Single +3.3 V Supply
- Common Receiver Enable Control
- High Impedance LVDS Inputs
- High Impedance Output Capability
- Temperature Range: -55°C to 125°C
- Input Common Mode Range: 0.05V to 2.35V
- Maximum Operating Frequency: 100MHz
- Minimum Input Differential Signal: 100mV

Low Power

The HXLVDSR dissipates less than 500mW with all outputs toggling at a data rate of 100MHz.

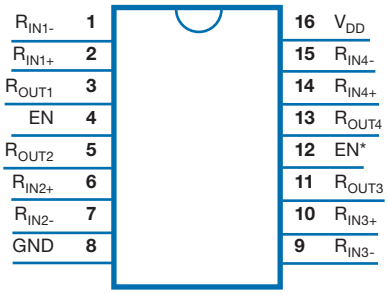
Common Receiver Enable Control(EN, EN*)

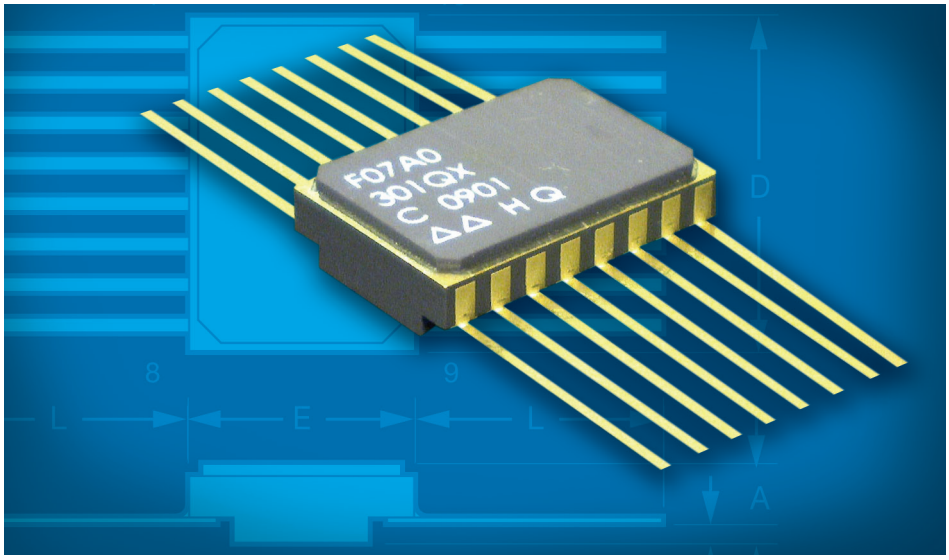
The EN and EN* inputs allow the user to put the digital outputs into high impedance mode.

Space Qualified Package

The HXLVDSR is packaged in a 16 lead ceramic flat pack.

Package Pinout





The HXLVDSR is a radiation hardened quad differential line receiver. It features four independent receivers with common receiver enable control and high impedance outputs. The high impedance output capability allows multiplexing outputs.

The HXLVDSR along with the HXLVDSD provide an alternative to high power devices for high speed point to point interface applications. The receivers are equipped with a wide (0.05V to 2.35V) common mode input voltage range.

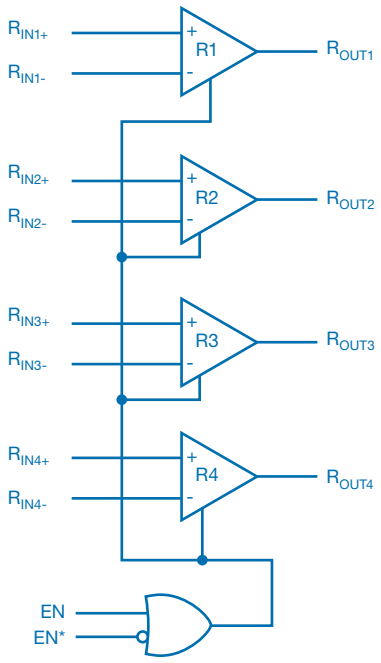
The HXLVDSR is manufactured on a radiation hardened SOI-IV Silicon On Insulator (SOI) process with very low power consumption.

The input of the HXLVDSR allows for easy interfacing to space and military imaging, sensor, and communications systems.

Pin Description

Pin	Symbol	Signal Type	Buffer Description
1	R_{IN1-}	I	LVDS
2	R_{IN1+}	I	LVDS
3	R_{OUT1}	OZ	CMOS 15mA
4	EN	I	CMOS
5	R_{OUT2}	OZ	CMOS 15mA
6	R_{IN2+}	I	LVDS
7	R_{IN2-}	I	LVDS
8	GND	GND	ground (V_{SS} = 0V)
9	R_{IN3-}	I	LVDS
10	R_{IN3+}	I	LVDS
11	R_{OUT3}	OZ	CMOS 15mA
12	EN*	I	CMOS
13	R_{OUT4}	OZ	CMOS 15mA
14	R_{IN4+}	I	LVDS
15	R_{IN4-}	I	LVDS
16	V_{DD}	PWR	supply voltage

Block Diagram



Truth Table

ENABLES EN	ENABLES EN*	INPUT RIN+ - RIN-	OUTPUT ROUT
L	H	X	Z
H	X	VID ≥ 0.1 V	H
X	L	VID ≥ 0.1 V	H
H	X	VID ≤ -0.1 V	L
X	L	VID ≤ -0.1 V	L

Signal Definition

EN, EN*

These are the common enable control signals. As shown in Truth Table, the combination of EN = L and EN* = H puts the outputs into the high impedance state. The outputs are enabled for all other combinations of EN and EN*.

R_{IN1} – R_{IN4}

These are LVDS differential input pins.

R_{OUT1} – R_{OUT4}

These are the 3.3V CMOS output pins.

Functional Description

The HXLVDSR is a radiation hardened quad differential line receiver designed for applications requiring low power dissipation and high data rates. The HXLVDSR accepts low voltage differential input signals and translates them to 3.3V CMOS output levels. The receiver includes high impedance output capability to allow multiplexing outputs. The EN and EN* inputs allow active Low or active High control of the high impedance outputs. The enable signals are common to all four receivers. The dual enable scheme allows for flexibility in turning devices on or off. The HXLVDSR along with the HXLVDSD provide an alternative to high power devices for high speed point to point interface applications.

Absolute Maximum Ratings (1)

Parameter	Symbol	Conditions	Limits Min	Limits Max	Units
Supply Voltage	V_{DD}	—	-0.5	+4.6	V
DC Input Voltage	R_{IN+}, R_{IN-}	—	-0.5	V_{DD}+0.5	V
DC Output Voltage	R_{OUT}	—	-0.5	V_{DD}+0.5	V
Enable Input Voltage	(EN, EN*)	—	-0.5	V_{DD}+0.5	V
Input Diode Clamp Current	I_{IK}	$V_{IN} < 0 - V_{TH\_diode}$ or $V_{IN} > V_{DD} + V_{TH\_diode}$	-42	+42	mA
Output Short Circuit Current (2)	I_{OS}	1 second, R_{OUT} shorted to GND or V_{DD}	-256	+200	mA
DC Output Current, Per Pin	I_O	R_{OUT} = 0 to V_{DD}	-50	+50	mA
Maximum Continuous Current Per Output Pin	—	—	-29.2	+29.2	mA
Thermal Resistance, Junction to Case	θ_{JC}	—	—	+16.3	°C/W
Storage Temperature Range	T_{STG}	—	-65	+150	°C
Lead Temperature (Soldering, 10 sec)	T_{LMAX}	—	—	+300	°C
Junction Temperature	T_J	—	—	+175	°C
ESD (Human Body Model)	—	—	—	2000	V

(1) Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
(2) One output at a time should be shorted and the max junction temperature should not be exceeded.

Recommended Operating Conditions (1)(2)

Parameter	Symbol	Limits Min	Limits Max	Units
Supply Voltage	V_{DD}	3.0	3.6	V
Case Temperature	T_C	-55	+125	°C
High Level Input Voltage, (CMOS Inputs)				
VDD = 3.0 V to 3.6 V	V_{IH}	$0.7V_{DD}$	—	V
Low Level Input Voltage, (CMOS Inputs)				
VDD = 3.0 V to 3.6 V	V_{IL}	—	$0.3V_{DD}$	V
Input Voltage (LVDS inputs)	V_{IN_LVDS}	0 V	+2.4	V
Input Voltage (CMOS inputs)	V_{IN_CMOS}	-0.3	V_{DD}+0.3	V
Output Voltage	V_{OUT}	-0.3	V_{DD}+0.3	V

(1) Specifications listed in datasheet apply when used under the Recommended Operating Conditions unless otherwise specified.
(2) All unused CMOS inputs must be held at ground or VDD. All unused LVDS inputs must be held at ground or 2.4 volts differentially.

Electrical Requirements

Conditions unless otherwise specified: 3.0 V ≤ VDD ≤ 3.6 V, -55°C ≤ TC ≤ +125°C, VSS = 0 V

Parameter	Symbols	Conditions	Limits Min	Limits Max	Units
Differential Threshold (LVDS Inputs)	V_{ID}	V_{CM} = 0.05V and 2.35V, V_{DD} = 3.0V	-100	100	mV
Common-Mode Voltage Range (LVDS Inputs) (2)	V_{CMR}	V_{ID} = 100 mV, peak to peak	0.05	2.35	V
Input Current High (LVDS Inputs)	I_{IH1}	V_{IN} = 2.4 V, V_{DD} = 3.6 V	-10	+10	µA
Input Current Low (LVDS Inputs)	I_{IL1}	V_{IN} = 0 V, V_{DD} = 3.6 V	-10	+10	µA
Output High Voltage (CMOS Outputs)	V_{OH}	I_{OH} = -15.0 mA, V_{DD} = 3.0V	2.5	—	V
Output Low Voltage (CMOS Outputs)	V_{OL}	I_{OL} = 15.0 mA, V_{DD} = 3.0V	—	0.5	V
Output Disable Current (CMOS Outputs)	I_{OZL}	Disabled, V_{OUT} = 0 V, V_{DD} = 3.6V	-10	+10	µA
	I_{OZH}	Disabled, V_{OUT} = V_{DD}, V_{DD} = 3.6V	-10	+10	µA
Input High Voltage (CMOS Inputs)	V_{IH}	EN and EN*, V_{DD} = 3.6V	—	2.52	V
Input Low Voltage (CMOS Inputs)	V_{IL}	EN and EN*, V_{DD} = 3.0V	0.9	—	V
Receiver Input Voltage Range V_{ia} or V_{ib} (LVDS Inputs) (1)	V_i		0	2.4	V
Input Current High (CMOS Inputs)	I_{IH2}	V_{IN} = V_{DD}, Other Inputs = 2.4V or GND differentially, EN & EN* only, V_{DD} = 3.6V	-10	+10	µA
Input Current Low (CMOS Inputs)	I_{IL2}	V_{IN} = GND, Other Inputs = 2.4V or GND differentially, EN & EN* only, V_{DD} = 3.6V	-10	+10	µA
No Load Supply Current, Receiver Enabled (static mode, LVDS inputs are not toggled)	I_{DD}	V_{DD} = 3.6V, EN, EN* = V_{DD} or GND, V_{IN+} = 0 V, V_{IN-} = 2.4V	—	47	mA
No Load Supply Current, Receiver Disabled	I_{DDSB}	V_{DD} = 3.6V, EN = GND, EN* = V_{DD}, V_{IN+} = 0 V, V_{IN-} = 2.4V	—	5	mA
Dynamic Supply Current		V_{DD} = 3.6 V, all outputs toggling , Cload = 85pF			mA
	I_{DDOP1}	1 MHz	—	86	
	I_{DDOP2}	10 MHz	—	94	
	I_{DDOP3}	50 MHz	—	126	
	I_{DDOP4}	100 MHz	—	136	

(1) Guaranteed but not tested.
(2) The VCMR range is reduced for larger V_{ID}.

Capacitance Parameters (1)

Parameter	Symbols	Conditions	Limits		Units
			Min	Max	
Input Capacitance (LVDS Inputs, with respect to ground)	C_{LI}		—	11	pF
Input Capacitance (CMOS Inputs, Receiver and package capacitance)	C_{CI}		—	12	pF
Output Capacitance (CMOS Outputs)	C_{CI}		—	12	pF

(1) Guaranteed but not tested.

Radiation-Hardness Ratings (1)

Parameter	Symbol	Environment Conditions	Limits	Units
Total Dose	TID		300	krad(Si)
Transient Dose Rate Upset	DRU	Pulse width ≤ 20ns	$1x10^9$	rad(Si)/s
Dose Rate Survivability	DRS	Pulse width ≤ 20ns	$1 x10^{12}$	rad(Si)/s
Neutron Fluence		1MeV equivalent energy	$1 x10^{14}$	N/cm^2

(1) Device will not latch up due to any of the specified radiation exposure conditions.

Radiation Characteristics

Total Ionizing Dose Radiation

The device radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Transient Dose Rate Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. The device will maintain basic functional operation during exposure to a pulse up to the DRU specification. The device will meet functional, timing and parametric specifications after exposure to a pulse up to the DRS specification.

Neutron Irradiation Damage

SOI CMOS is inherently tolerant to damage from neutron irradiation. The device meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup

The device will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

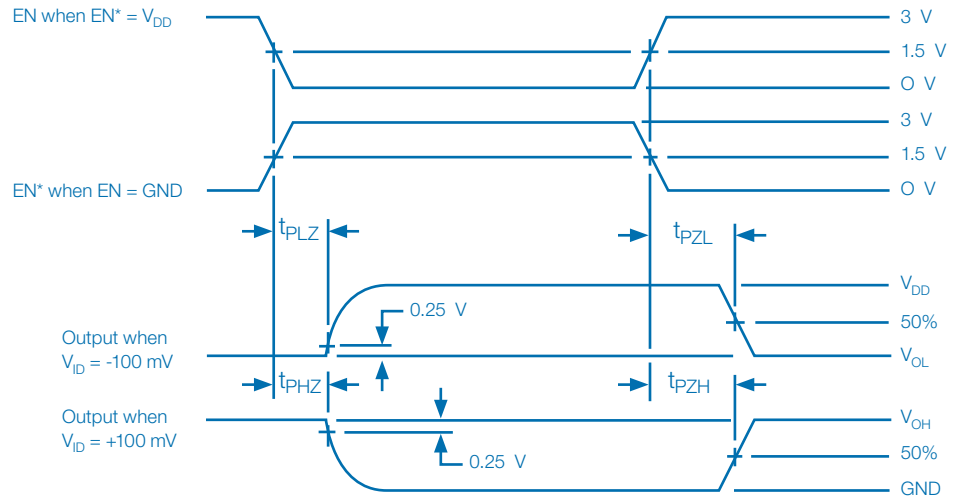
Switching Parameters

Test Conditions unless otherwise specified: 3.0 V ≤ VDD ≤ 3.6 V, -55°C ≤ TC ≤ +125°C, VSS = 0 V

Parameter	Symbols	Conditions	Limits Min	Limits Max	Units
Receiver output jitter (1)(2)	t_{PWD1}	Clock	—	15	ps
Receiver output jitter with power supply distortion (1)(2)(3)	t_{PWD2}	Clock	—	350	ps
Receiver output jitter (1)(2)	t_{PWD3}	Data	—	1600	ps
Receiver output jitter with power supply distortion (1)(2)(3)	t_{PWD4}	Data	—	1800	ps
Differential Propagation Delay High to Low	t_{PHLD}	CL = 10 pF, VID = 200 mV, input transition time < 3.0ns	1.8	6.6	ns
Differential Propagation Delay Low to High	t_{PLHD}	input pulse = 1.1 V to 1.3 V, VIN = 1.2V (0V differential) to VOUT = 1⁄2 VDD, CL = 10pF, input transition time < 3.0ns	1.8	7.4	ns
Differential Pulse Skew | tPHLD - tPLHD | (1)(4)	t_{SKD}	C_L = 10 pF, V_{ID} = 200 mV	—	1.3	ns
Differential Channel-to-Channel Skew-same device (1)(5)	ΔSK_{CC}	C_L = 10 pF, V_{ID} = 200 mV	—	1.3	ns
Differential Part to Part Skew (1)(6)	ΔSK_{PP}	C_L = 10 pF	—	2.2	ns
Differential Part to Part Skew (1)(7)	ΔSK_{PP}	C_L = 10 pF	—	2.9	ns
Output Rise Time, 20%-80% of signal swing (1)	t_R	C_L = 10 pF	—	1.5	ns
Output Fall Time, 20%-80% of signal swing (1)	t_F	C_L = 10 pF	—	1.2	ns
Disable Time High to Z (8)	t_{PHZ}	See $V_{OUT} = V_{OH}$-0.25V	—	13.6	ns
Disable Time Low to Z (8)	t_{PLZ}	Timing $V_{OUT} = V_{OL}$+0.25V	—	12.7	ns
Enable Time Z to High (8)	t_{PZH}	diagram V_{OUT} = 50%	1.8	17	ns
Enable Time Z to Low (8)	t_{PZL}	V_{OUT} = 50%	1.8	17	ns
Operating Frequency	f_{MAX}	All channels switching, t_{RISE} and t_{FALL} <1.0ns, load = 10pF	—	100	MHz

(1) Guaranteed but not tested by vendor.
(2) Maximum LVDS Receiver Jitter performance is guaranteed between -5°C and 125°C case temperature, between 3.0 V and 3.6 V; and pre- and post-radiation.
(3) AC sine wave Power Supply Noise of 60 mV p-p applied at 25 MHz.
(4) The skew is the absolute value of the difference between the differential propagation delay High to Low and the differential propagation delay Low to High of the same channel.
(5) The skew is the channel-to-channel difference of the differential propagation delays for any event on the same device.
(6) The skew is the absolute value of the difference between the minimum and maximum differential propagation delays between devices. Devices must be at the same VDD and within 5°C of each other.
(7) The skew is the absolute value of the difference between the minimum and maximum differential propagation delays between devices.
(8) Cload = 10pF

Timing Diagrams

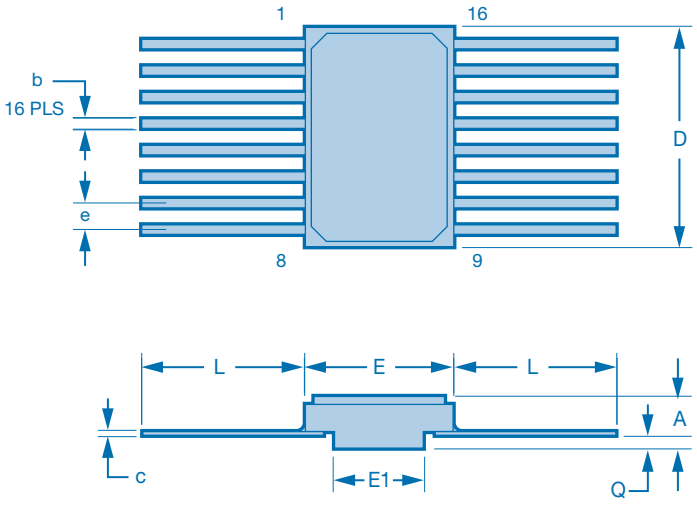


Signal Integrity

As a general design practice, for digital input signals, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns.

Floating inputs for an extended period of time is not recommended.

Package Outline Dimensions



Symbol	Dimensions - Inches Min	Dimensions - Inches Max	Dimensions - Millimeters Min	Dimensions - Millimeters Max
A	.101	.125	2.57	3.18
b	.015	.019	0.38	0.48
c	.004	.007	0.11	0.18
D	.392	.408	9.96	10.36
e	.047	.053	1.20	1.34
E	.274	.286	6.96	7.26
E1	.185	.196	4.70	4.96
L	.320	.360	8.13	9.14
Q	.022	.032	0.56	0.82

Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

Screening and Conformance Inspection

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

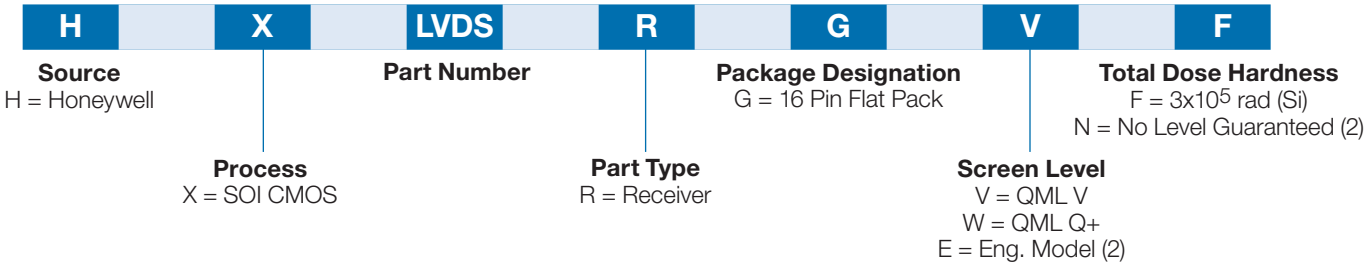
Conformance Summary

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

Ordering Information

Standard Microcircuit Drawing

The HXLVDSR can be ordered under the SMD drawing 5962-07A03.



(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 for further information.
(2) Engineering Device Description: Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation hardness guaranteed. Screen Level and Total Dose Hardness codes must be “E” and “N” respectively.

QCI Testing (1)

Classification	QCI Testing
QML Q+	No lot specific testing performed. (2)
QML V	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell Quality Management Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Find out more

To learn more about Honeywell’s radiation hardened integrated circuit products and technologies, visit www.honeywellmicroelectronics.com/

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ADS-14204 Rev A
June 2014