Honeywell

HTOP01 Die Deliverable

High Temperature Dual Precision Operational Amplifier

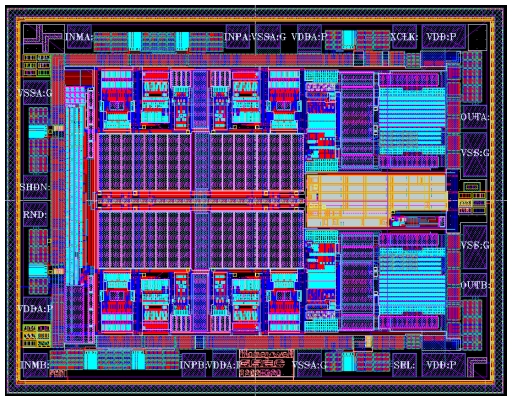
DESCRIPTION

The HTOP01 is a precision low power op amp, offering very low input offset voltage and drift over an operating temperature range of -55°C to 225°C. Using auto-zeroing techniques input offset voltage is continuously sampled and compensated, providing near perfect offset voltage compensation over temperature and time.

An internal oscillator and logic provides all necessary auto-zero clock signals, and no external capacitors are needed.

The internal auto-zero clock generator produces a pseudo-random clock frequency operating between 2kHz – 4kHz that effectively "spreads out" the clock noise frequency spectrum over a 2kHz span. This greatly reduces detectable clock noise in the amplifier's output spectrum.

Additionally, an external clock input pin (XCLK) is provided along with a select input pin (SEL) to choose between the internal clock and an optional external clock.



The external clock option allows timing flexibility for synchronously sampled systems, where no clock energy can be tolerated in the sampled amplifier output.

To save power, a power shutdown pin (SHDN) de-powers all analog circuitry when asserted (active high). The current with SHDN asserted is <150μA over temperature.

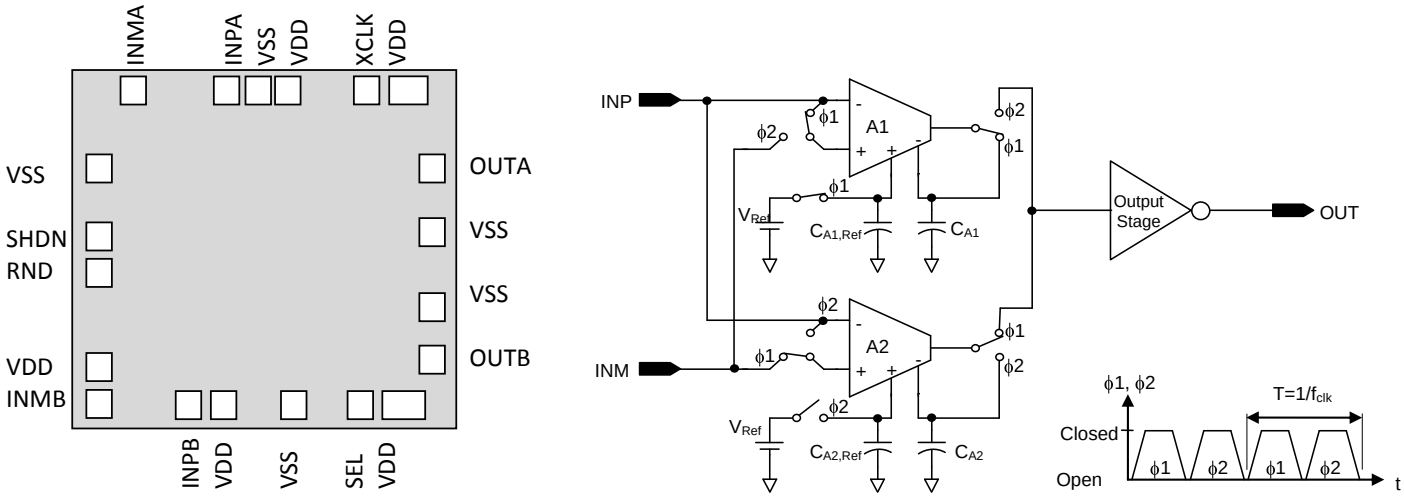
APPLICATIONS

Downhole Drilling Measurement and Production Tools
Strain Gauge Transducers
RTD Temperature Sensing
High Temperature Instrumentation
High Resolution Data Acquisition
Low Power Measurement

FEATURES

- -55^{O}C to 225^{O}C Ambient Temperature Range
- Continuous Input Offset Voltage Auto-Zeroing With Internal Clock
- Input Offset Voltage: ±100μV Max Over Temperature
- Input Offset Drift: 0.2μV/^{O}C Max
- High Gain, CMRR: 100dB Min
- Gain-Bandwidth Product: 2.0MHz Typical
- Single 5V Supply Operation
- 5.0mA maximum Supply Current
- Power shutdown pin provided
- External clocking option for synchronous systems

DIE PAD AND FUNCTIONAL BLOCK DIAGRAM



SIGNAL DESCRIPTION

Pin Name	Description
SEL	Digital input pin. Selects either internal clock (SEL=0) or externally applied clock (SEL=1).
XCLK	Digital input pin. External clock input. When SEL=1, XCLK is enabled, and the internal ping-pong amplifier action occurs on each XCLK edge. When SEL=0, XCLK is disabled. When not used, XCLK should be connected to VDD or VSS.
SHDN	Digital input pin. Power Shutdown control input. When SHDN=1, all analog circuitry is de-powered/disabled, and only leakage current will flow into VDD. When SHDN=0, normal circuit operation occurs.
INPA, INPB	Non-inverting amplifier inputs for amplifier “A” and “B” respectively.
INMA, INMB	Inverting amplifier inputs for amplifier “A” and “B” respectively.
OUTA, OUTB	Amplifier “A” and “B” outputs.
VDD	Positive supply connection.
VSS	Negative supply connection.
RND	Honeywell Test Pin Only. Connect to VDD for normal operation. When connected to ground the clock randomization will be turned off.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating		Units
		Min	Max	
VDD	Supply Voltage (2)	-0.5	6.5	Volts
VPIN	Voltage on Any Pin (2)	-0.5	VDD+0.5	Volts
TSTORE	Storage Temperature	-65	300	°C
IOUT	Average Output Current		50	mA
ESD	Electrostatic Discharge Protection Voltage (3)	1000		V

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) Class 2 Electrostatic Discharge (ESD) input protection voltage per MIL-STD-883, Method 3015 on the package part.

RECOMMENDED OPERATING CONDITIONS (1)

Symbol	Parameter	Description			Units
		Min	Typ	Max	
VDD	Supply Voltage	4.5	5.0	5.5	Volts
TC	External Package Temperature	-55	25	225	°C
Temp Op	Operating Temperature	-55		225	°C
VPIN	Voltage on Any Pin	-0.3		VDD+0.3	Volts

(1) Voltages referenced to Vss.

ELECTRICAL CHARACTERISTICS

V_{DD}=5V, V_{SS} =0V unless otherwise noted. Values apply over the full –55°C to 225°C ambient temperature range except where denoted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	SEL=0 (Internal Clock) See Note 6			100	µV
ΔV_{OS}	Average Input Offset Voltage Drift				0.2	µV/°C
I_B	Input Bias Current	T_A = 25°C T_A = -55°C to +225 °C See Note 1		±10	±50 ±150	pA nA
I_{OS}	Input Offset Current	T_A = 25°C T_A = -55°C to +225 °C See Note 1		±10 ±1		pA nA
e_n	Input Noise Voltage	RS=100Ω, 0.1Hz – 10Hz (internal clock) 25°C (internal clock) 225°C (External clock at 30KHz) 25°C		5.7 4.6 1.4		µV pk-pk µV pk-pk
I_R	Input Range		V_{SS}		V_{DD} - 2.0	Volts
CMRR	Common Mode Rejection Ratio	VCM = 0V to V_{DD} – 2.0V (Measured at DC)	100			dB
PSRR	Power Supply Rejection Ratio	V_{SS} = 0, 4.75V ≤ V_{DD} ≤ 5.25V (Measured at DC)	90			dB
A_{VOL}	Large Signal Voltage Gain	RL = 10kΩ (Measured at DC)	100			dB
GBWP	Gain-Bandwidth Product	RL = 10kΩ, CL = 20pF		2.0		MHz
SR	Slew Rate	RL = 10kΩ		1.5		V/µs
	Overload Recovery Time	RL = 10kΩ CL = 20pf Positive Negative		140 35		µs
I_O	Output Current	Output swings (V_{DD}-0.3V) – (V_{SS}+0.3V) See Note 2	±20			mA
I_{OSC}	Output Short-Circuit Current	Output shorted to V_{DD}, V_{SS} See Note 4		±50		mA
f_{CLK}	Clock Frequency	Internally generated clock. See Note 5		2 - 4		kHz
V_{DD} - V_{SS}	Operating Supply Range		4.75		5.25	Volts
I_{SUP}	Supply Current, Total Package	See Note 3			5.0	mA
V_{IH}	Digital Input High Voltage	Applies to XCLK, SEL, SHDN pins	V_{DD} – 0.3		V_{DD} + 0.1	Volts

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Digital Input Low Voltage	Applies to XCLK, SEL, SHDN pins	V_{SS} – 0.1		V_{SS} + 0.3	Volts
I_{SHDN}	Supply Current w/SHDN asserted	SHDN=1			150	µA

Notes

(1) As temperature increases, current into the op amp inputs becomes dominated by leakage current from the input protect diodes. At 250°C junction temperature, diode leakage current can reach ±100nA when the input level is near VDD or VSS. Net leakage current drops significantly as the input level approaches mid-rail, and is at a minimum when the input level is precisely midway between VDD and VSS.

Additionally, the diode structures on each input are well matched to each other, and will exhibit nearly identical leakage current behavior. Consequently, offset current IOS between the two inputs is typically about ±1% of the IB level. Thus, if the input level is maintained near mid-rail, IOS is very low (<|1nA|), even at 250°C junction temperature.

(2) Output drive current capability is related to output swing magnitude. The HTOP01 will sink and source 20mA minimum over temperature with the output swinging to within 300mV of either rail. At lesser loads, the output can swing closer to the supply rails; at loads of ≤1mA, the output will reach to within ~10mV of either rail. For applications where the output remains ≥500mV away from the rails, up to ±40mA output current is available. Current limiting activates when output current exceeds approximately ±50mA.

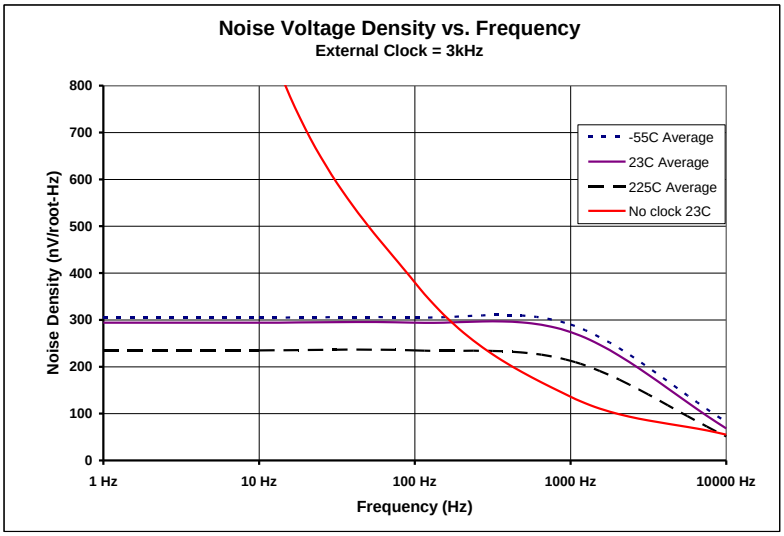
(3) Supply current consumed by each op amp is PTAT (Proportional To Absolute Temperature) in nature, and as the name suggests increases proportional to temperature. The 5.0mA maximum current given in the table reflects the maximum current consumed at 250°C junction temperature by both amplifiers. At 25°C junction temperature, supply current is typically 2mA. PTAT biasing maintains a near-constant amplifier bandwidth over temperature, a desirable characteristic.

(4) The HTOP01 is designed to handle ±50mA output current per amplifier continuously over temperature, with no reduction in rated product life. In the event of an overload condition, current limiting activates and limits output current to ~50mA nominally. However, due to fabrication process variations, the current limiting threshold can vary up to ±30%. Consequently, it is possible to have a current limiting threshold as high as ~65mA. In this situation, if the overload (65mA) is allowed to continue indefinitely at 225°C ambient, there can be a reduction in rated product life. For maximum product life, it is recommended that any overload output current situation (>50mA) be attended to promptly.

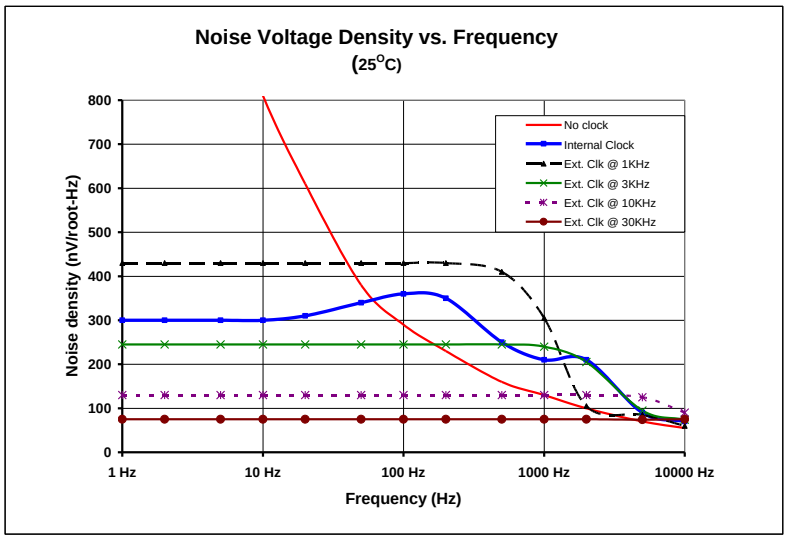
(5) The pseudo-random amplifier auto-zero clock is derived from an on-chip oscillator running at a nominal frequency of 4.0MHz.

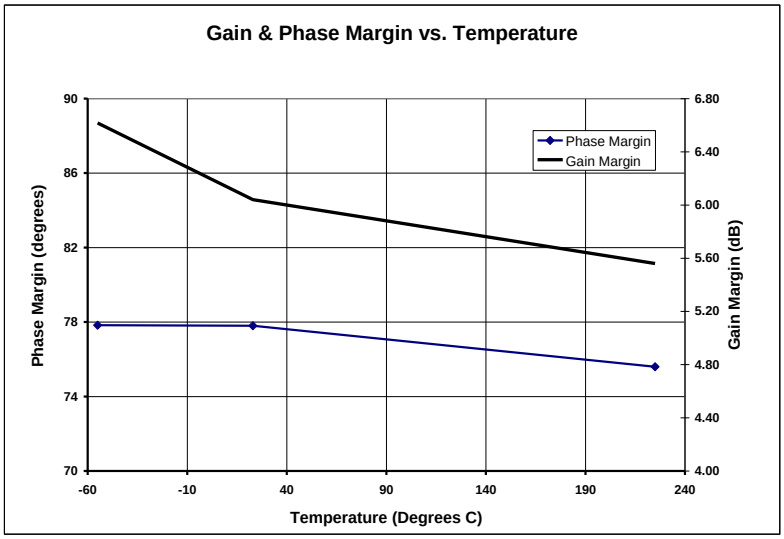
(6) With SEL=0 the HTOP01 uses an internally generated clock for offset compensation. Setting SEL=1 and using an external clock provides superior offset performance over the internal clock. The recommended frequency range for an external clock is from 4KHz to 100KHz. Optimum performance is achieved with an external clock frequency of approximately 30KHz.

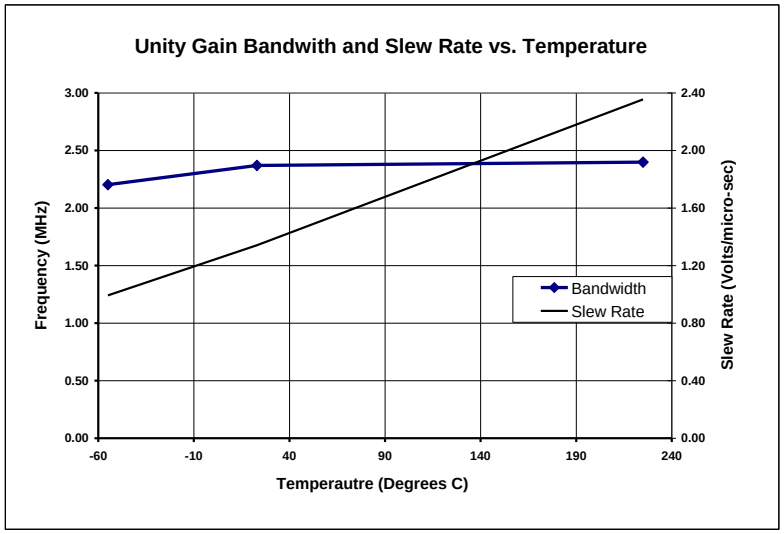
TYPICAL PERFORMANCE PLOTS



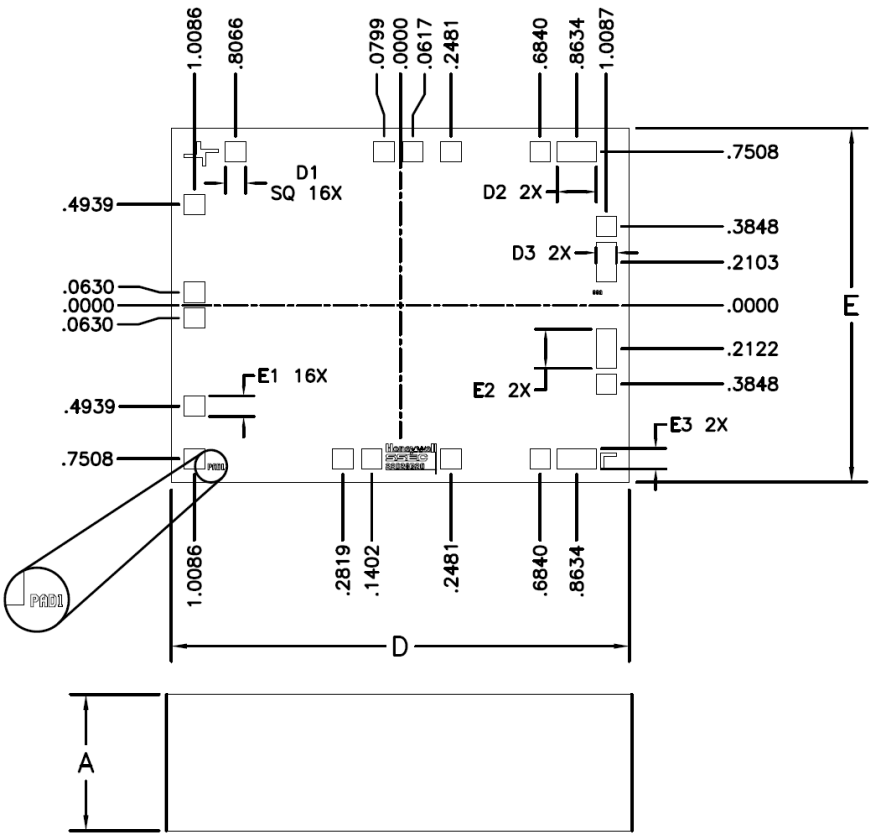
TYPICAL PERFORMANCE PLOTS







DIE OUTLINE



SYMBOL	COMMON DIMENSIONS MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.655	0.675	0.695
D	---	---	2.242
E	---	---	1.732
D1	---	.100	---
E1	---	.100	---
D2/E2	---	.192	---
D3/E3	---	.100	---

Notes:
(1) Backside metalization is gold.
(2) Metalization on the pads is aluminum.
(3) The backside of the die is connected to VSS.

ASSEMBLY RECOMMENDATIONS

Die Bonding

Honeywell recommends using a Eutectic Gold/Silicon perform or Cyanate Ester adhesive for die bonding to a ceramic package.

Wirebonding

Aluminum wire shall be used for wirebonding. The power and ground pads shall be wirebonded before the other signal pads.

APPLICATION NOTES

1. SUPPLY BY-PASS CAPACITANCE

In order to minimize the effects of supply-coupled clock noise on amplifier output it is recommended that a supply by-pass capacitor with low equivalent series resistance be connected between VDD and VSS.

2. INPUT IMPEDANCE MATCHING

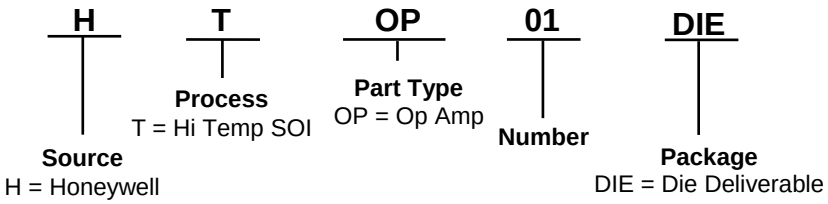
At high temperature input currents into the HT0P01 will increase due primarily to leakage of the input ESD protection diodes. It is therefore helpful to minimize and/or balance input impedance to avoid voltage offsets from input current flowing in external connections.

DIE LEVEL SCREENING

The HTOP01 die are specified to operate over the entire temperature range. To meet this objective, three levels of screening are in place.

1. Wafer Level – Each die is 100% electrical tested at room temperature.
2. Sample Package Test – A sample of die from each wafer are assembled into packages and screened over the temperature range of -55C to +225C to verify performance.
3. The sample packaged parts also receive 48 hours of burn-in at 250C.

ORDERING INFORMATION (1)



SHIPPING CONTAINER

The HTOP01DIE die will be shipped in waffle packs.

Find out more

For more information on Honeywell's High Temperature Electronics visit us online at www.honeywell.com/hightemp, or contact us at 800-323-8295 or 763-954-2474. Customer Service Email: ssec.customer.service@honeywell.com.

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