HMXDAC01

Honeywell

Radiation Hardened 12-Bit, Monolithic D/A Converter

Features

- Monolithic 12-Bit D/A Converter
- Rad Hard: 300k Rad(Si) Total Dose
- Single +5 V Analog Supply
- 5V or 3.3V Digital and I/O Supply
- Offset Error: < ±0.3% FSR
- Offset Temperature Coefficient: < ±50PPM of FSR/°C
- Gain Error: < ±5% FSR
- Gain Temperature Coefficient: < ±150 PPM of FSR/°C
- Integral Nonlinearity Error: < ±4 LSB
- Differential Nonlinearity Error: < ±1 LSB
- Settling Time to 1LSB: < 1.4µs
- Full Scale Range: 0mA to 5mA (0V to 2V range for 400 ohm load resistor)
- Power Supply Rejection Ratio PSRR: < ±0.35 %FSR/V

- **Mixed Signal Rad Hard Process**

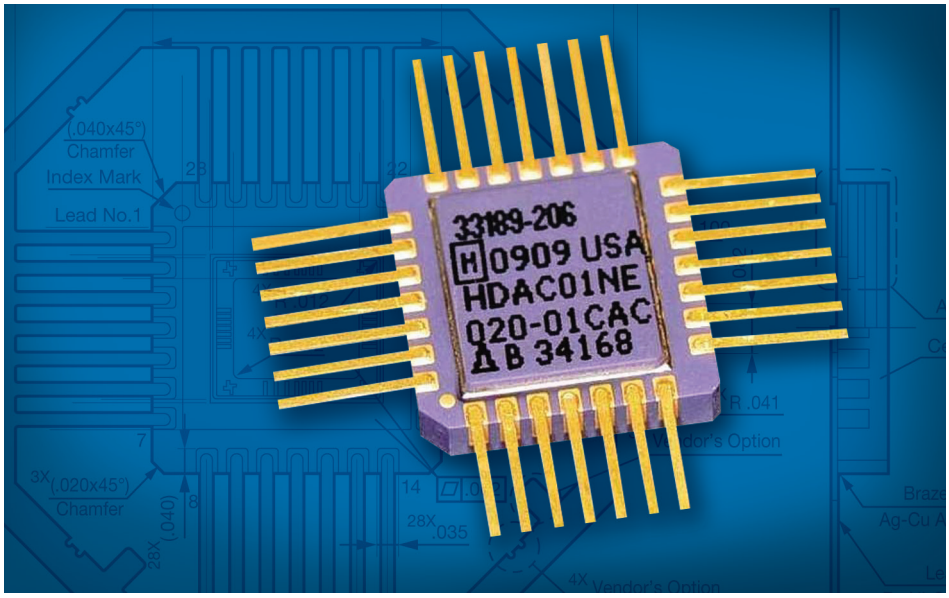
  The HMXDAC01 is fabricated on space qualified SOI CMOS process. High-speed precision analog circuits are now combined with high-density logic circuits that can reliably withstand the harshest environments.

- **Dual Power Supply Capability**

  The HMXDAC01 operates on two power supplies. The analog supply is 5V and the digital IO is 3.3V.

- **Space Qualified Package**

  The HMXDAC01 is packaged in a 28 lead quad ceramic flat pack.



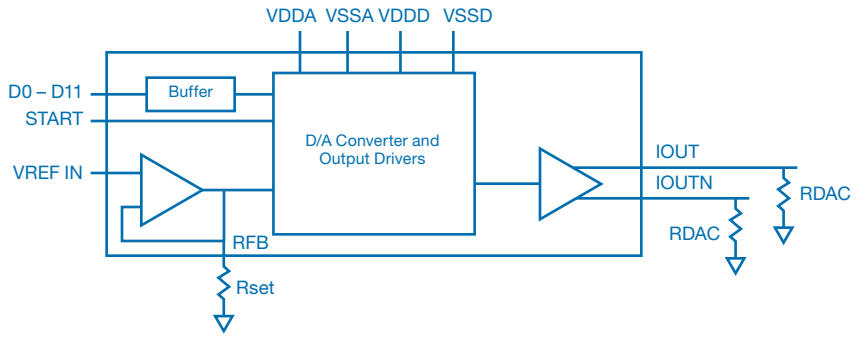
The HMXDAC01 is a radiation hardened monolithic, 12-bit, differential current steering digital-to-analog converter. It is a 6 x 2 x 4 doubly segmented architecture with the six MSBs linearly decoded and the four LSBs binary decoded. The intermediate two bits are linearly decoded. The six MSBs employ a two dimensional hierarchical symmetrical switching sequence to compensate and average two dimensional matching errors.

The HMXDAC01 is fabricated on radiation hardened SOI-IV Silicon On Insulator (SOI) CMOS process with very low power consumption.

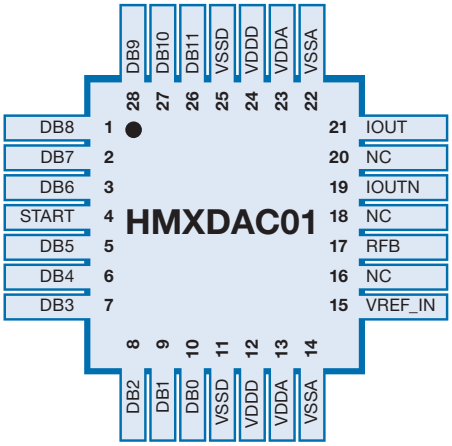
The input of the HMXDAC01 allows for easy interfacing to space and military imaging, sensor, and communications systems.

A single clock input is used to control all internal conversion cycles.

Simplified Functional Block Diagram



Pinout Diagram



Pin Description

Pin	Pin Name	Description
1	DB8	Data Bit 8
2	DB7	Data Bit 7
3	DB6	Data Bit 6
4	START	Clock Input
5	DB5	Data Bit 5
6	DB4	Data Bit 4
7	DB3	Data Bit 3
8	DB2	Data Bit 2
9	DB1	Data Bit 1
10	DB0	Data Bit 0 (LSB)
11	VSSD	Digital Ground
12	VDDD	Digital Supply Voltage
13	VDDA	Analog Supply Voltage
14	VSSA	Analog Ground
15	VREF_IN	Bias Control
16	NC	No Connect
17	RFB	Feedback Resistor Input, (Rset to GND)
18	NC	No Connect
19	IOUTN	Remainder Output Current, (RDAC to GND)
20	NC	No Connect
21	IOUT	Output Current, (RDAC to GND)
22	VSSA	Analog Ground
23	VDDA	Analog Supply Voltage
24	VDDD	Digital Supply Voltage
25	VSSD	Digital Ground
26	DB11	Data Bit 11 (MSB)
27	DB10	Data Bit 10
28	DB9	Data Bit 9

Signal Definition

Name	Description
DB0-DB11	The digital data input pins control the value of the output current. DB11 is the most significant bit (MSB) and DB0 is the Least Significant Bit (LSB).
START	This is the clock signal which initiates a conversion. The positive going edge latches in the data present on the DB0-DB11 pins.
VREF_IN	This is the reference voltage input pin. A 2V reference voltage is required by the circuit.
IOUT	This is the output current. This will be in the range of 0mA to 5mA based on the 12 bit input code. This pin is normally connected through a RDAC resistor to ground. The value of RDAC is suggested to be 400Ω. This value of RDAC will give an output voltage range of 0V to 2V.
IOUTN	This is the remainder of the full scale current specified by the 12 bit input code. This pin is normally connected through a RDAC resistor to ground.
RFB	This is the feedback resistor pin. A feedback resistor Rset is required to be connected from GND to the RFB pin. The typical value for Rset is 25.59 +/- .01% Kohms.

Absolute Maximum Ratings (1)(2)

Parameter	Symbol	Limits Min	Max	Units
Analog Supply Voltage (3)	VDDA	-0.5	6.5	Volt
Digital Supply Voltage (3)	VDDD	-0.5	6.5	Volt
Power Dissipation	P_D		150	mW
Vref Input Voltage (3)(4)	VREF_IN	-0.5	VDDA+0.5	Volt
Vref Input Current (4)		-50	50	mA
Digital Input Voltage (3)(4)	DB0 – DB11, START	-0.5	VDDD+0.5	Volt
Digital Input Current (4)	IDB0 – IDB11, ISTART	-50	50	mA
Thermal Resistance, Junction to Case (5)	θ_{JC}		8.1	°C /W
Junction Temperature	T_J		175	°C
ESD Human Body Model (Handling/Manufacturing)			500	V
Lead Temperature (Soldering, 10 seconds)	T_{LMAX}		300	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
(2) VSSA=VSSD = 0 volts
(3) Absolute maximum value not to exceed 6.5 V.
(4) Input and output terminals are diode clamped to the power supply rail and ground. Input and output signals that can swing more than 0.5 volts beyond the power supply rails should be current limited to 50mA or less.
(5) By analysis.

Recommended Operating Conditions (1)(2)

Parameter	Symbol	Limits Min	Max	Units
Clock Frequency		>0	3	MHz
Analog Supply Voltage	VDDA	4.75	5.25	V
Digital Supply Voltage	VDDD	3.135	3.465	V
Bias Control	VREF_IN	1.998	2.002	V
Case Operating Temperature	T_C	-55	125	°C
Feedback Resistor	Rset	25	26	Kohms
IOUT Resistor	RDAC	399.6	400.4	ohms

(1) All voltages are with respect to VSSA = VSSD = 0.0 volts.
(2) Specifications listed in datasheet apply when used under the Recommended Operating Conditions unless otherwise specified.

Functional Description

The HMXDAC01 is a 12 bit differential current steering DAC. It is a 6x2x4 doubly segmented architecture with the six MSBs linearly decoded and the four LSBs binary decoded. The intermediate two bits are linearly decoded.

The total output current available from the DAC is 5mA. Based on the digital input code, a fraction of the 5mA is steered to the IOUT pin while the remaining portion of the 5mA is steered to the IOUTN pin. In order to convert the current output into a voltage output, an external resistor is required. A resistor, RDAC, needs to be connected from IOUT to ground and from IOUTN to ground. A value of 400Ω for RDAC will give an output voltage range of 0V to 2V. The full scale current output is determined by Rset and Vref as described by the following equations:

Iref = Vref/Rset

Iout (full scale) = 64*Iref => 5 mA

Radiation Characteristics

Total Ionizing Dose Radiation

The device radiation hardness assurance TID level was qualified by ^{60}Co testing per MIL-STD-883 Method 1019 with the exception of overdose and accelerated anneal. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Transient Dose Rate Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. The device will maintain basic functional operation during exposure to a pulse up to the DRU specification. The device will meet functional, timing and parametric specifications after exposure to a pulse up to the DRS specification.

Neutron Irradiation Damage

SOI CMOS is inherently tolerant to damage from neutron irradiation. The device meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup

The device will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

Radiation Hardness Ratings (1)

Parameter	Symbol	Environment Conditions	Limits	Units
Total Ionizing Dose, F-Level (2)	TID		$3x10^5$	rad(Si)
Transient Dose Rate Upset	DRU	Pulse width ≤ 20ns	$1x10^9$	rad(Si)/s
Transient Dose Rate Survivability	DRS	Pulse width ≤ 20ns	$1 x10^{12}$	rad(Si)/s
Neutron Irradiation		1 MeV equivalent energy	$1 x10^{14}$	N/cm^2

(1) Device will not latch up due to any of the specified radiation exposure conditions.
(2) Parts tested without accelerated annealing.

Electrical Requirements (1)

Rset=25.59KΩ, VREF_IN=2.0V, RDAC=400Ω , VDDA=5.0 +/- 5%, VDDD=3.3+/- 5%,VSSA=VSSD=0.0V, TC=-55 C to 125 C (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Max	Unit
Offset Error	OFFSET	see Note (2)	-0.3	0.3	%FSR
Gain Error	GAIN	see Note (2)	-5.0	5.0	%FSR
DC ACCURACY					
Integral Nonlinearity	INL	see Note (2)	-4.0	4.0	LSB
Differential Nonlinearity	DNL	see Note (2)	-0.99	0.99	LSB
Offset Temperature Coefficient	OFFSET_TC		-50	50	ppm of FSR/C
Gain Temperature Coefficient	GAIN_TC		-150	150	ppm of FSR/C
Settling Time for half scale code transition (±1 LSB)	t_{S1}		-	2.5	µS
Settling Time for 1/16th scale code transition (±1 LSB)	t_{S2}		-	1.4	µS
DAC Output Capacitance	C_{OUT}	(4)	-	15	pF
High Level Input Voltage (minimum)	V_{IH}	VDDD = 3.135V	2.31	-	V
Low Level Input Voltage (maximum)	V_{IL}	VDDD = 3.135V	-	.99	V
High Level Input Current	I_{IH}	VDDD = 3.465V, Vin = 3.465V	-20	20	µA
Low Level input Current	I_{IL}	VDDD = 3.465V, Vin = 0.0V	-20	20	µA
Analog Power Supply Current	I_{DDA}	bits = 1 $V_{IN} = V_{DDD}$, V_{DDD} = 3.465V, V_{DDA} = 5.25V	-	12.5	mA
Digital Power Supply Current	I_{DDD}	bits = 1 $V_{IN} = V_{DDD}$, V_{DDD} = 3.465V, V_{DDA} = 5.25V	-	6.25	mA
D.C. Differential	PSRR	VDDA = +4.75V to +5.25V			
PSRR		VDDD = 3.3 V (3)	-0.35	0.35	%FSR/V

(1) Monotonicity guaranteed by DNL test.
(2) Peak fit method is used on Offset Error, Gain Error, DNL and INL measurements.
(3) PSRR = (gain error at 5.25V – gain error at 4.75V) / (5.25 V – 4.75 V).
(4) Maximum capacitance is verified as part of initial qualification only.

Signal Integrity

As a general design practice, for digital input signals, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns.

Floating inputs for an extended period of time is not recommended.

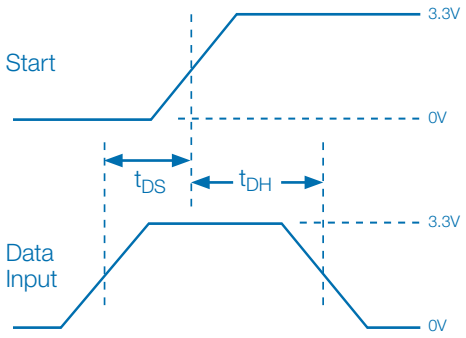
Timing Requirements

Rset=25.59KΩ, VREF_IN=2.0V, RDAC=400Ω (unless otherwise specified)

Timing Requirements	Symbol	Conditions	Limits Min	Limits Max	Units
Data Setup Time	TDS	See Timing Diagram	0	-	ns
Min Start Pulse	TPW	(1)	20		ns
Data Hold Time	TDH	See Timing Diagram	20		ns

(1) The rising edge of the start pulse generates an internal pulse that latches the input data. The start signal must go low before the start of another data conversion.

Timing Diagram



Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

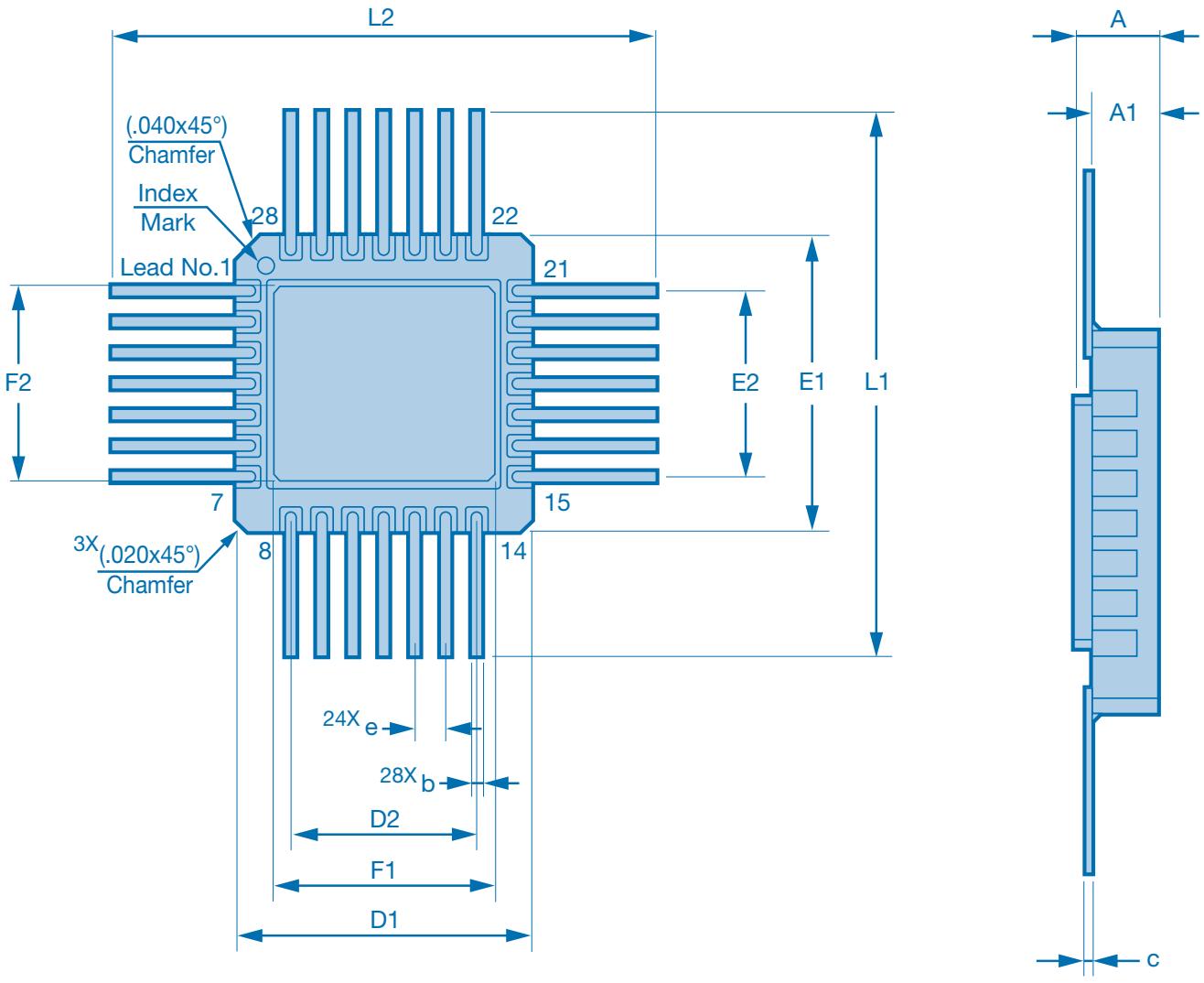
Screening and Conformance Inspection

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Conformance Summary

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

Package Outline Dimensions (1)

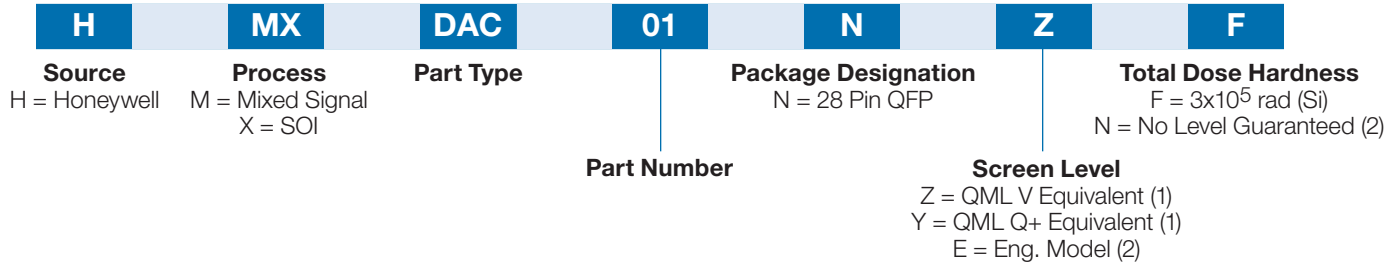


(1) Controlling dimensions are in inches.

(2) "A" is the height of the package including the lid.

Symbol	Dimensions - Inches			Dimensions - Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	.094	.106	.118	2.39	2.69	3.00
A1	.076	.085	.094	1.93	2.16	2.39
b	.017	.019	.021	0.43	0.48	0.53
c	.004	.005	.007	0.10	0.13	0.18
e	.045	.050	.055	1.14	1.27	1.40
D1/E1	.470	.478	.486	11.94	12.14	12.34
D2/E2	.295	.300	.305	7.49	7.62	7.75
F1	.354	.358	.362	8.99	9.09	9.19
F2	.312	.316	.320	7.92	8.03	8.13
L1/L2	—	—	.896	—	—	22.76

Ordering Information



(1) This is an equivalent screening flow but this device is not QML qualified.
(2) Engineering Device Description: Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation hardness guaranteed.

QCI Testing (1)

Classification	QCI Testing
QML Q+ and QML Q+ Equivalent	No lot specific testing performed. (2)
QML V and QML V Equivalent	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell Quality Management Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Find out more

To learn more about Honeywell's radiation hardened integrated circuit products and technologies, visit www.honeywellmicroelectronics.com/

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