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High Temperature Analog to Digital Converter Reliability Testing

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Outline / Motivation

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HTADC12 - High Temp 12-Bit ADC Reliability Study

- **It is common practice to characterize and compensate initial measurement errors in down-hole tools**
- **Component drift over time and temperature cycling are therefore just as important to know/predict as time-zero accuracy**
- **Parametric shifts affecting post-compensation accuracy are presented for a 12-bit ADC from samples stressed by 250°C bias plus temperature cycling from -65°C to 200°C**
- **Mechanical / Assembly data is also presented**

HTADC12 Block Diagram

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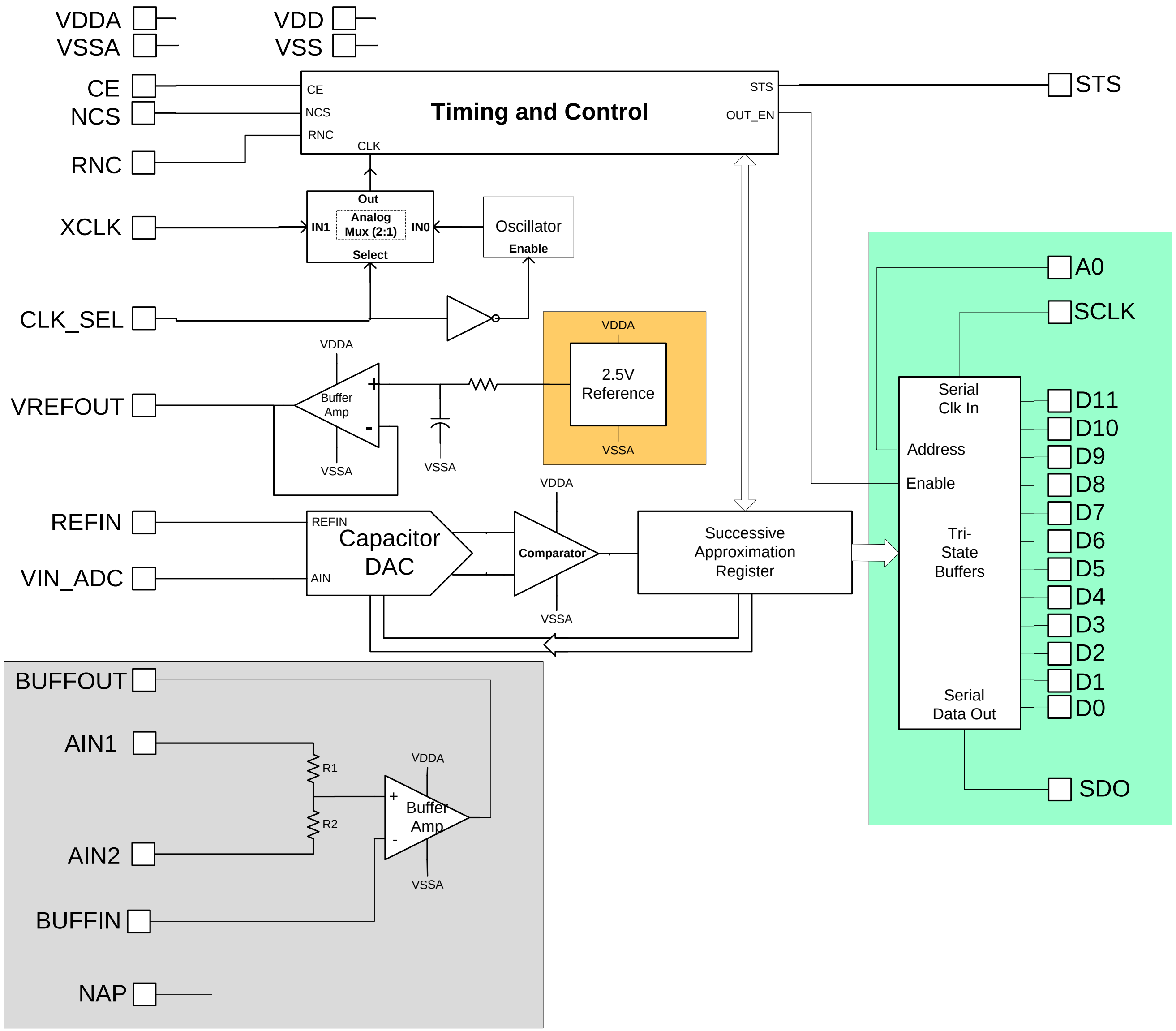

- **12 Bit Successive Approximation ADC**
- **Temperature range: -55°C to 225°C**
- **5V supply: 0V to VREF full-scale input range**
- **On-chip 2.5V Reference**
- **On-chip buffer op amp**
- **4MHz internal clock for conversion**
- **10µs conversion time**
- **Parallel or Serial data outputs**
- **28 or 14 pin DIP package configurations**

Life-test/Temp-Cycle/Test Flowchart

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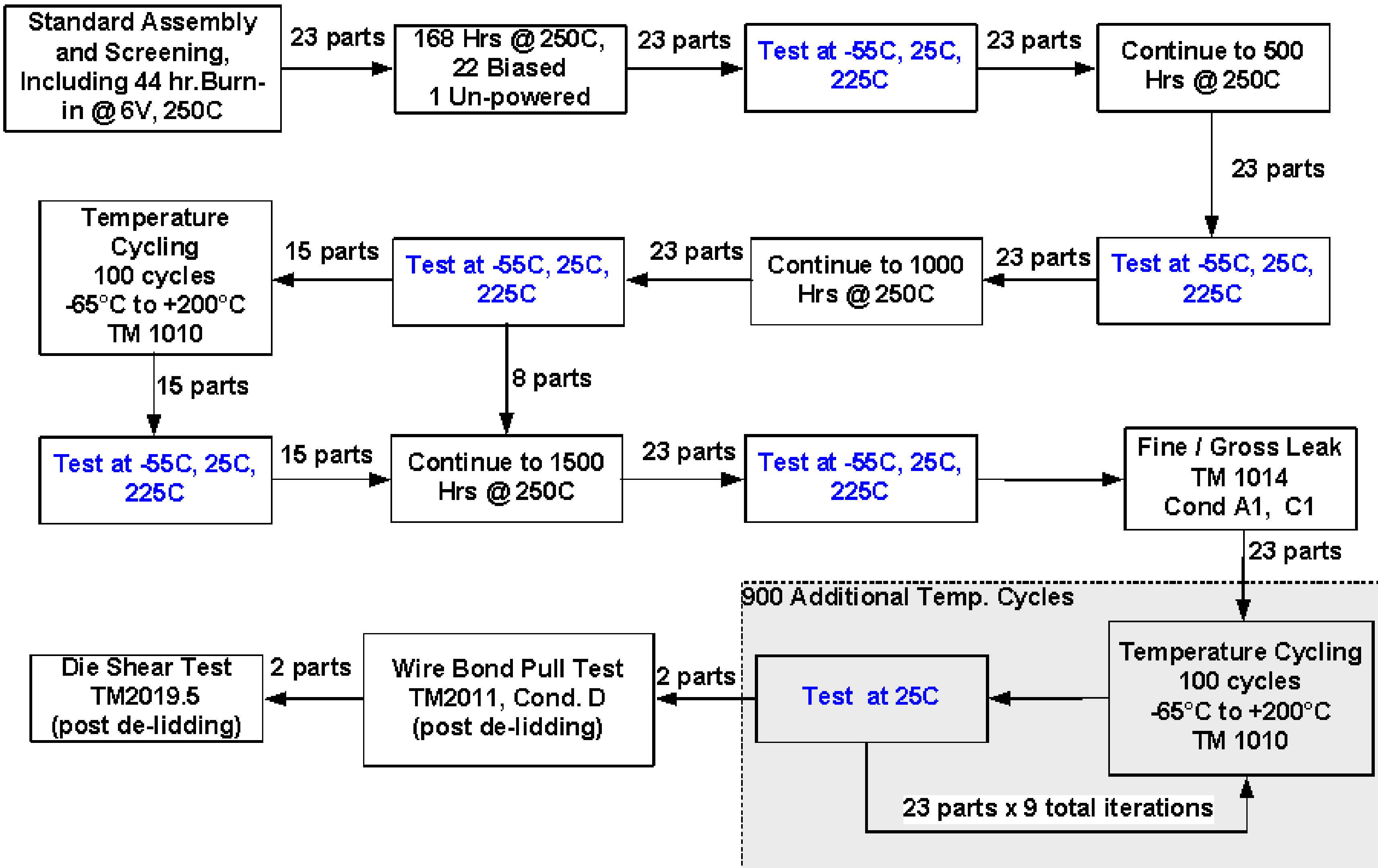
1500 Hours at 250C + 1000 Temp-cycles (-65°C to 200°C)



Assembly Details

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- **Ceramic 28-lead DIP package**
  - Multi-layer alumina ceramic
  - Kovar lid / Furnace seal
  - Alloy 42 side-brazed leads
  - Gold over nickel surface metalization
- **Gold-backed SOI die**
  - Die-size = 2.8mm x 2.9mm
  - Aluminum wirebond pads
- **Gold-eutectic die bond**
  - Gold (1% Si) die attach preform
- **Aluminum ultra-sonic wedge bond**
  - 1.25 mil aluminum (1.5% Si) wire

14-lead package uses similar materials/flow

Current production uses high-temp. adhesive die-attach

Life-test Fixture

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- High-temp. sockets mounted on aluminum rails.
- Wire-wound resistors
- Nickel wire/Fiberglass sheath
- Welded + Soldered connections (95/5 Pb/Sn solder)

Burn-in / Life-test Configuration

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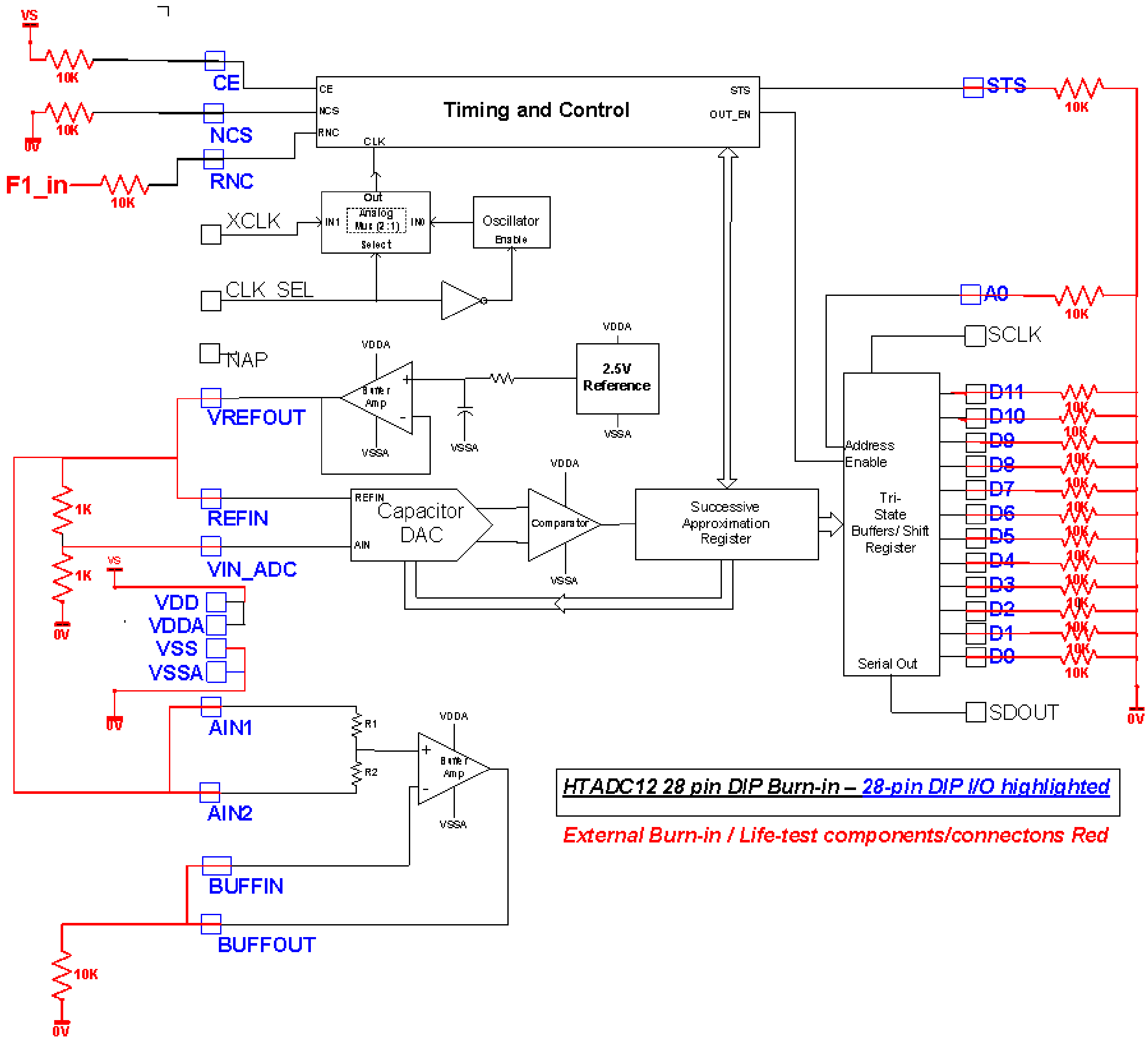
- **Configured for continuous conversion at Vin=half-scale**
- **Buffer Amp configured as voltage-follower with Vin=2.5V**
- **VDD = 6V (operating = 5V)**
- **Oven at 250°C**



HTADC12 28 pin DIP Burn-in – 28-pin DIP I/O highlighted

External Burn-in / Life-test components/connectons Red

Electrical Test Parameters

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- At each electrical test point collected data using automated tester
- On-chip temperature monitored by forward drop of ESD diodes
- Test program collects DC data:
  - Buffer Amplifier offset voltage at 2.5V VIN
  - ADC offset, full-scale, and linearity errors
  - Conversion Time: Controlled by on-chip R-C oscillator
  - No-load output of the 2.5V reference
    - *Conversion time and VREF tempco/scale-factor are trimmed at wafer test*

Note:

- **The ADC has superior INL/DNL performance at high temp relative to room temperature**
- **Cross-over from 1.1 to 2.0 LSB INL to 0.5 LSB INL is observed at »160°C**
- **This is attributed to design attributes rather than process/device stability**

225°C results provide best insight into performance and stability of the technology

Life-test results (225°C data)

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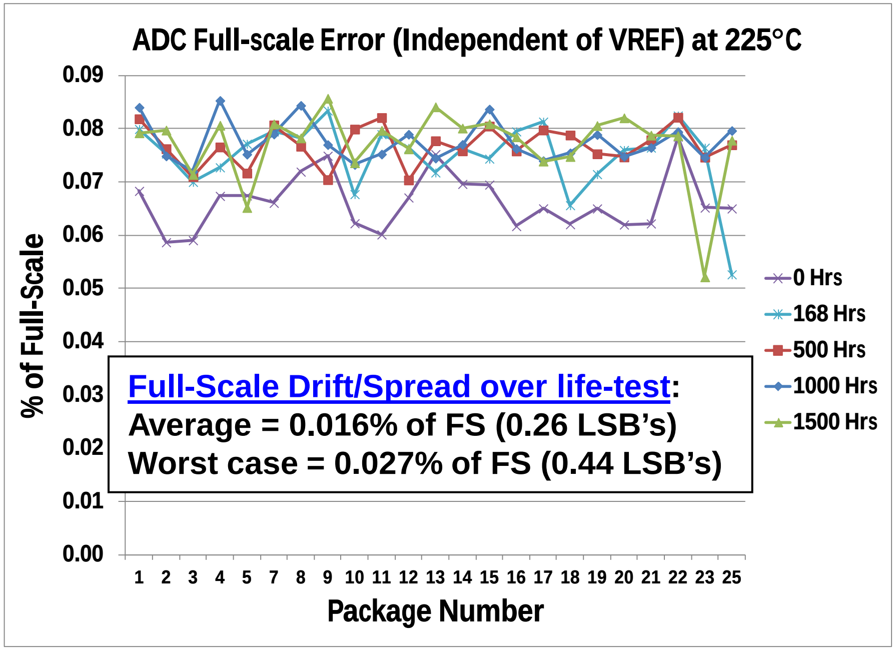

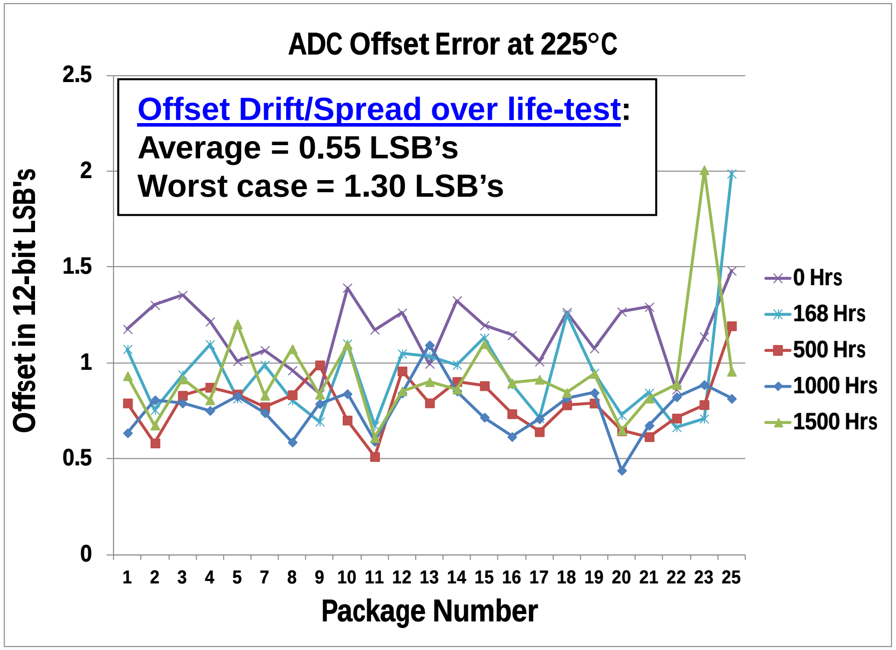

- **These results are obtained with an external reference applied (i.e., independent of any VREF drift)**
- **General trend:**
  - **Full-scale/Offset errors show an initial shift (within 168 hrs) in opposite directions**
  - **Indicative of an "end-point shift" in the transfer function**

Life-test Results (225°C data)

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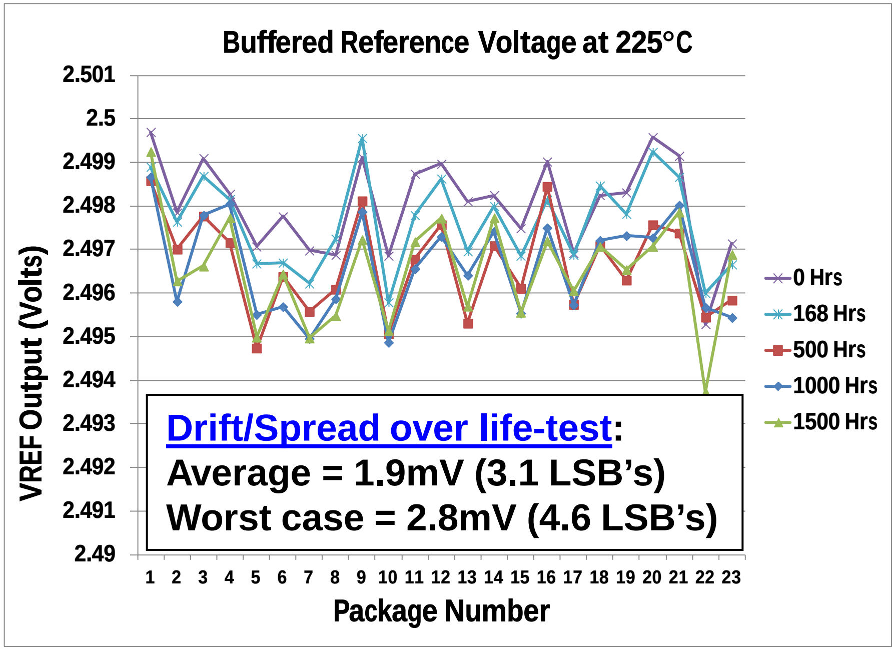

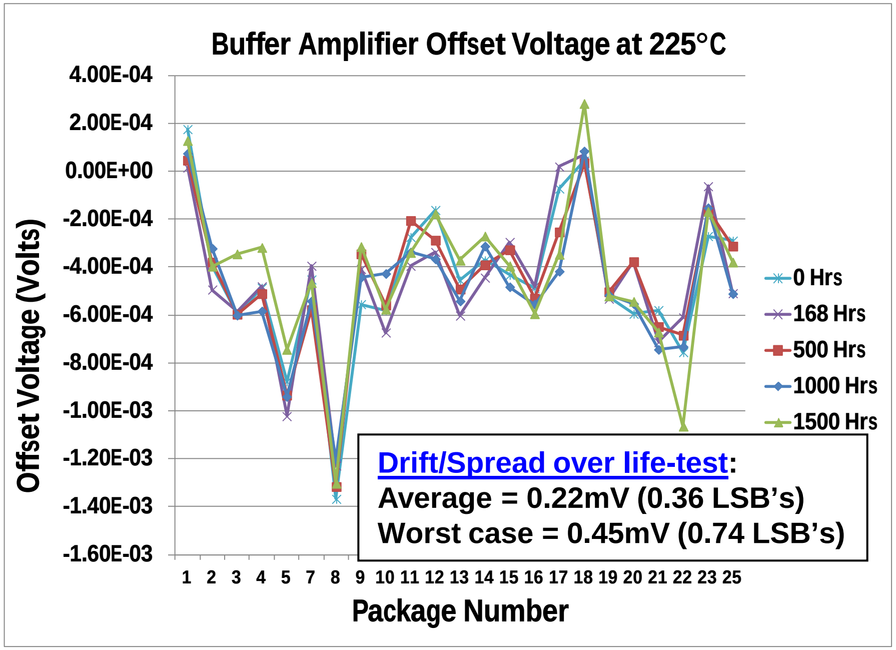

- **Buffered 2.5V reference is generally applied as the ADC Reference Input and defines the full-scale input range**
- **Buffer amplifier may be used to drive the ADC input**
  - **In that case shift in buffer amplifier offset adds to ADC offset**

Temp. Cycling Results (25°C Data)

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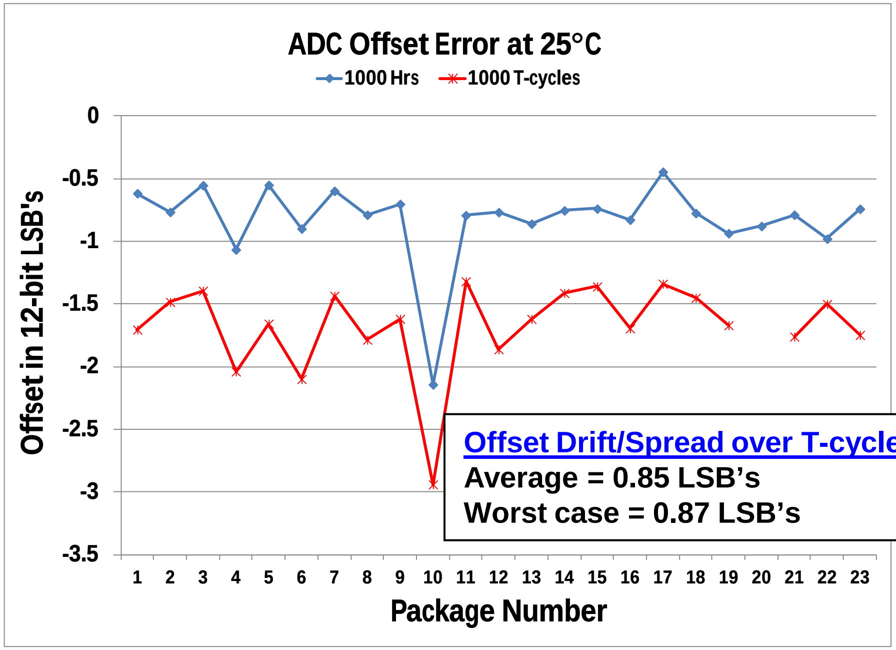
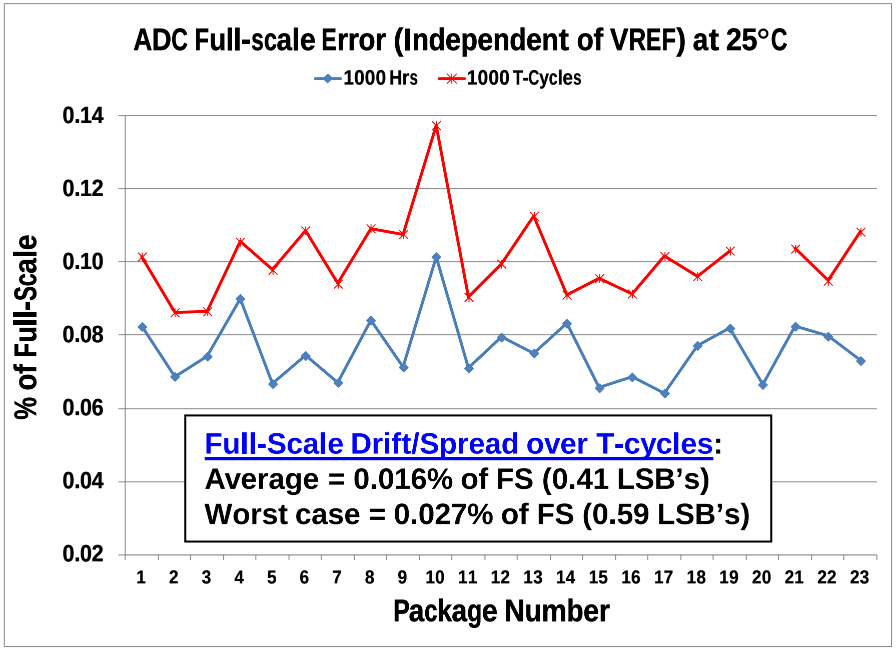


Offset Drift/Spread over T-cycles:
Average = 0.85 LSB's
Worst case = 0.87 LSB's



Full-Scale Drift/Spread over T-cycles:
Average = 0.016% of FS (0.41 LSB's)
Worst case = 0.027% of FS (0.59 LSB's)

- **Above charts compare data prior to T-cycling (blue) to data obtained after T-cycling (Red)**
- **Full-scale/Offset shifts in opposite directions are observed**
  - **Indicative of an "end-point shift" in the transfer function**

Integral Non-Linearity (INL) Results

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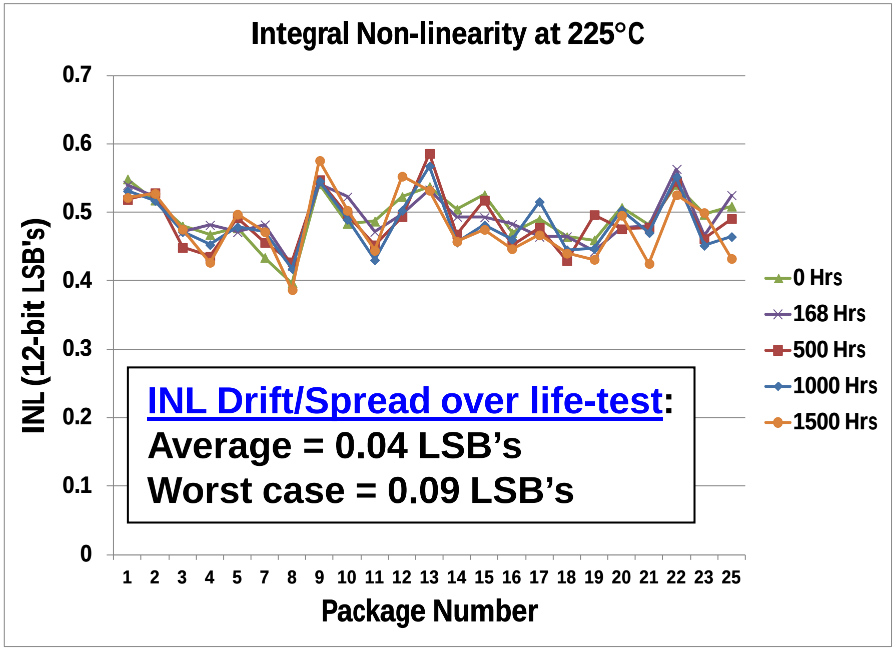

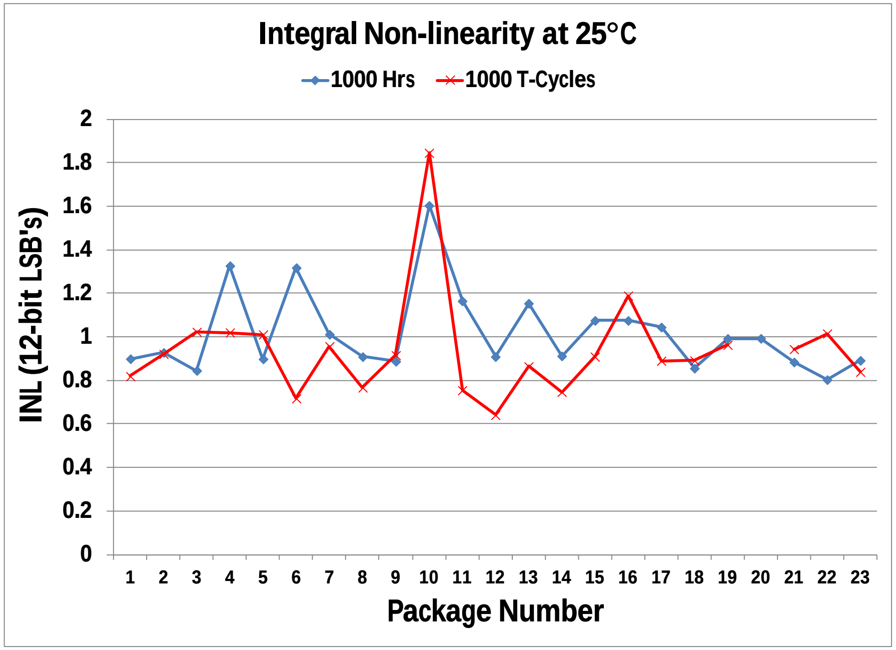

- **1500 hours at 250°C + 1000 T-cycles does not significantly change linearity**

Electrical Parameter Summary

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Predicted Accuracy Degradation from Results

	Typical	Worst-case	Units
Drift after 1500 hrs @ 250C			
ADC Offset and Full-scale	0.81	1.74	LSB's
Buffer Amplifier	0.36	0.74	LSB's
VREF	3.1	4.6	LSB's
Additional Drift from 1000 T-Cycles			
ADC Offset and Full-scale	1.26	1.46	LSB's
Total from above sources	5.53 0.14	8.54 0.21	LSB's % of FS

- Reference drift is dominant error source
- Followed by ADC Offset/Full-scale drift with temperature cycling
- Resolution/Linearity is not significantly impacted

Mechanical / Assembly Test Results

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- **All parts passed hermeticity tests**
  - Mil-Std 883, TM1014, conditions A1, C1
  - 1500 Hours at 250C, 100 Temperature Cycles (-65°C, 200°C)
- **Wire-bond pull tests passed**
  - Mil-Std 883, TM1011, condition D
  - 1500 hrs @ 250C, 1000 T-cycles
  - 2 packages, 70 wires pulled
  - Ave. pull-strength = 5.7 grams, Minimum = 4.9 grams
  - Pass criteria is 2.0 grams
- **Die-shear tests passed**
  - Mil-Std 883, TM1019
  - 2-die tested : 23.3 kgf / 30.2 kgf shear strength
  - Pass criteria is 1.0 kgf

Summary and Conclusion

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- **Testing has been completed to provide benchmark data/results for predicting ADC performance over time at high temp. with temperature cycling**
- **Mechanical integrity, functionality, and linearity are stable over the test conditions**
  - **1500 Hours at 250C, 1000 Temperature Cycles (-65°C, 200°C)**
- **Total compensated accuracy degradation is 5.5 LSB's typical (3.3mV for a 2.5V full-scale range)**
  - **Dominated by reference voltage drift**
- **Potential for marginal improvement from extended burn-in/pre-conditioning**

Honeywell High Temperature Website

www.hightempsolutions.com

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