An SOI Precision Reference and Bias Circuitry for Operation to 250°C

Bruce W. Ohme and Mark R. Larson

Honeywell International Inc.
Honeywell Aerospace, Defense & Space
12001 State Highway 55, Plymouth, Minnesota 55441

Phone: 763-954-2189, Fax: 763-954-2742
E-mail: bruce.ohme@honeywell.com

Abstract

An SOI precision voltage reference has been developed and verified that provides a buffered, low-noise output well suited for general purpose high temperature and/or wide temperature range applications. The reference provides 0.3% accuracy from 25℃ to 225℃, with rms output noise of less than 5μV at 225℃. This reference was designed for use as a reference source for high-resolution A-to-D converter. The reference is buffered to provide up to 5mA source/sink capability and is adjustable via external components and a feedback pin. Associated with the reference on the same die are bias and utility functions. These include Proportional to Absolute Temperature (PTAT) current-mode and voltage-mode thermometer outputs and reference current sources. A wide variety of applications and temperature compensation schemes can be supported by this combination of functions in a single component. The reference uses lateral bipolar transistors fabricated in an SOI CMOS using the standard CMOS layout layers. This work has been performed within the Department of Energy DeepTrek Program with the participation of industry partners in a Joint Industrial Participant (JIP) program.

Key words: High-temperature electronics, EEPROM, FPGA, Analog-to-Digital Converter, Amplifier

1.0 Introduction

In extended temperature range electronic systems there is almost always a requirement for a temperature stable reference voltage (or current source). In any system involving sensors, it is also very useful to have access to voltage and/or current sources with linear temperature dependence, either as a means of measuring temperature, biasing the sensors, or for temperature compensation or scaling of the sensor response.

CMOS has long been the work-horse of the integrated circuit industry. CMOS designs have long exploited approaches adapted from earlier bipolar technologies for integrated voltage references. Most integrated circuit references are based on bipolar devices, including those implemented in CMOS processes [1]. For extreme high-temperature applications (>200°C) Silicon-on-Insulator (SOI) CMOS is generally required. Lateral bipolar transistors have been used to develop high-temperature SOI band-gap reference circuits [2-6].

This paper describes a general purpose SOI CMOS voltage reference and bias circuits. This circuit is embedded within a high-resolution A-to-D converter. The A-to-D converter is being developed with the U.S. Department of Energy's DeepTrek program, administered by the Strategic Center for Natural Gas (SCNG), at the National Energy Technology Laboratory [7-9]. The key features of this circuit block have been specified by industrial partners collaborating with DOE on the project.

For this application, a buffered voltage reference is needed, capable of fast-settling when sampled by the input structure of the A-to-D's sigma-delta modulator. The reference also must have very-low 1/f noise. Beyond that, the industrial partners working on this program were keen to have features and outputs beyond what is strictly required to service the A-to-D. This arises from other applications within the system and the fact that high-temperature stable and/or linear reference components are not generally available. Hopefully these additional features will serve to maximize the utility of this development.

Deep Trek program industrial partners are Baker Hughes, BP America, Goodrich Aerospace,

Honeywell, Intelliserv, Quartzdyne, and Schlumberger.

2.0 Design Application and Objectives

A block diagram of the reference and bias block that has been developed is provided in Figure 1. The features that have been included can be described in terms of some of the potential applications which they may serve. As Figure 1 shows, there is a basic voltage reference (VREF) block. As will be described later, within this block is a band-gap circuit that employs lateral PNP transistors. Inherent in this approach is the development of a Proportional-to-Absolute-Temperature (PTAT) current. These two signals, a temperature stable voltage and a linear temperature-dependent current are buffered and/or combined to provide the primary outputs of the circuit.

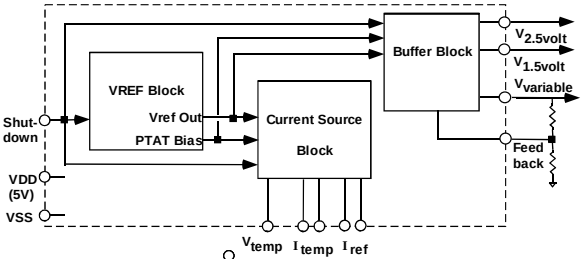

Figure 1: Reference and Bias Block Diagram

The buffer-block (on the right in Figure 1) has three voltage-mode outputs. The first of these is a 2.5V fixed-voltage ($V_{2.5Volt}$). This is a buffered source with active push-pull output that can nominally source or sink 5mA. It has current-limiting feature on the output with a nominal short-circuit current of ±30mA. In this project this output serves as the full-scale reference for an auxiliary 8-bit A-to-D converter, but can also be used off-chip. For example, it has sufficient drive capability to bias resistive pressure, temperature, or magnetic sensors. It can also provide a convenient mid-supply reference for differential analog sensing and control topologies in a 5V-suppy system.

The second voltage-mode output is a 1.5V fixed voltage ($V_{1.5Volt}$). This output has a source-follower output stage with limited current-sinking capability. It is intended to directly drive the reference input for a high-resolution (18-bit) over-sampled A-to-D converter. It is required to settle to less than 0.5 LSB (3μV) of its final value within 5μsec when sampled onto a 10pF load. This reference must also have very low 1/f noise (less than 1 LSB in the 0.1 to 50Hz band).

The third voltage-mode output is a variable reference output ($V_{Variable}$) that can be scaled by external resistors to any value from1.5V to 4.5V. This has an output stage similar to the fixed 2.5V output, and can likewise actively source/sink current and has short-circuit current limiting. This is a general-purpose, low-noise buffered reference. It is ideally suited for driving bridge type transducers.

All three voltage-mode outputs are referenced from a common reference source; they all track one another over temperature and aging. They are therefore well-suited to applications such as bridge transducers where bridge bias and full-scale reference are scaled versions of a common reference. With this type sensing and measurement configuration it is possible to develop measurement systems that (to first order) are independent of reference variations.

The "Current Source Block" in Figure 1 provides primarily current-mode outputs. However, the first output discussed is actually a voltage-mode output. It is the output labelled "V_{temp}" and is a thermometer output (i.e., a voltage-mode temperature signal). In precision applications, especially those involving wide-temperature range, it is often useful (or necessary) to know the local ambient temperature so that temperature-compensating means may be applied for offsets and non-linearity in the measurement system. The V_{temp} output is specified to provide a temperature signal that nominally traverses from 0V to 2.5V as the temperature ranges from -55°C to +285°C.

The remaining outputs are current-source outputs. There are two temperature-scaled current sources (labelled I_{tmep1} and I_{temp2}). Both of these are nominally specified to be 8μA at room temperature. I_{temp2} is specified to be a true PTAT output. Given that the nominal design target is 8μA at 298°K, then it follows that the temperature sensitivity of this current is approximately 40nA/°C. PTAT bias sources can be very useful in electronics systems. For example, amplifiers biased with PTAT currents achieve a very good over-all trade-off between gain, bandwidth, and common-mode range over a wide temperature span. Another use of PTAT current sources is to apply the output to a temperature stable resistor, yielding a PTAT voltage that can be scaled by the resistor value.

One shortcoming of a strictly PTAT signal for many applications is that it's full dynamic range

includes temperatures that are not useful (i.e., extremely cold). What is preferable in most cases is a signal that is Proportional-to-Reference-Temperature (PTRT). That is the intent of I_{temp1}. I_{temp1} is nominally specified to have an output of 0μA at a temperature of -55°C, the minimum specified temperature range of this application. The scale factor on this output is nominally 100nA/°C.

Finally there is a "Shutdown" control signal in Figure 1. Many of the high-temperature system applications targeted by the Deep Trek program use batteries and therefore power management is critical to extending mission life. The shut-down control provides means for putting all of the VREF and bias circuitry into a low-power state when operation is not required. This is generally done by shutting off bias current sources.

A summary of some of the key design targets/features of the VREF and bias block is provided in Table 3 below.

TABLE 3: Design Targets

Parameter	Target Value
Supply voltage	5V ± 5%
Variable reference output voltage range	1.5V to 4.5V
Temperature Variation: 0°C to 225°C	1.1% max.
Output noise, 0.1Hz to 10 Hz	15μV rms (max).
Constant-current outputs	200μA, typ.
Current source matching	±2%
Constant-current source temperature variation: 0°C to 225°C	2.3% max.
Temperature scaled current sources: 25°C output I_{temp1} output I_{temp2} output Temperature scale factor I_{temp1} output I_{temp2} output	 8μA 8μA 0.1μA/°C 0.04μA/°C (PTAT)
V_{Temp} Thermometer voltage -55°C output 25°C output 285°C output	 0.0V 0.6V 2.5V

4.0 Implementation

4.1 Lateral PNP Devices in SOI

A multi-purpose high-temperature SOI CMOS process has been used on this project [10-12]. In this process the standard P-channel MOS transistor may be used as a lateral PNP transistor (see Figure 2). The source, body, and drain terminals function as emitter, base, and collector. The gate of the MOS transistor is typically biased in accumulation so that there is not any complication from the "parasitic" PMOS action. This results in a device that has low 1/f noise relative to a standard MOS device.

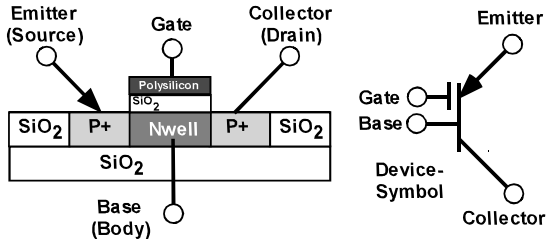

Figure 2: Lateral PNP Structure and Device Symbol

Due to the relatively large base width (MOS gate length, 0.8 microns in this process) and the high resistance of the base, this is not a high performance bipolar transistor. It is sufficient for operation at relatively low currents and serves for band-gap voltage circuits.

An advantage of SOI technology in this regard is the fact that all the terminals of the bipolar transistor may be connected independently and there are no parasitic devices as in some bulk CMOS processes (for example, reference [1]).

4.2 Bandgap Reference

A simplified schematic of the band-gap reference block is provided as Figure 3. This circuit employs lateral PNP transistors. It is based on generating a PTAT voltage (ΔVbe) by forcing equal currents to flow in the 1x and 8x PNP transistors. The 8x transistor is eight times larger than the 1x device and therefore is biased at lower current density. The difference in base-emitter voltage between bipolar transistors operated at different current densities is given by the familiar equation:

$$\Delta Vbe = \ln A \bullet (kT/q)$$

"A" is the ratio of current density in the 1x device relative to the 8x device. In the circuit configuration shown, ΔVbe is impressed across R1, and therefore to the extent that R1 is temperature invariant (or at least linear with temperature) the current flowing in R1 is PTAT.

Equal currents are forced in the 8x / 1x pair by the feedback loop established by OTA1,

M1 and the current mirrors. Note that ΔVbe is amplified by the ratio of R4 to R1 before being applied at the input to OTA1. This topology is a key to reducing the 1/f noise of the reference. The noise of OTA1 referred back to the "input" (ΔVbe) is attenuated by this gain. OTA1 is implemented as a folded-cascode transconductance amplifier with Pch input and uses very large input devices as well as N-channel loads to maintain low 1/f noise and low offset voltage. Although not shown, it is worth noting that the current mirrors are implemented using lateral PNP transistors to take advantage of the much lower 1/f noise of these devices relative to standard PMOS cascode current mirrors.

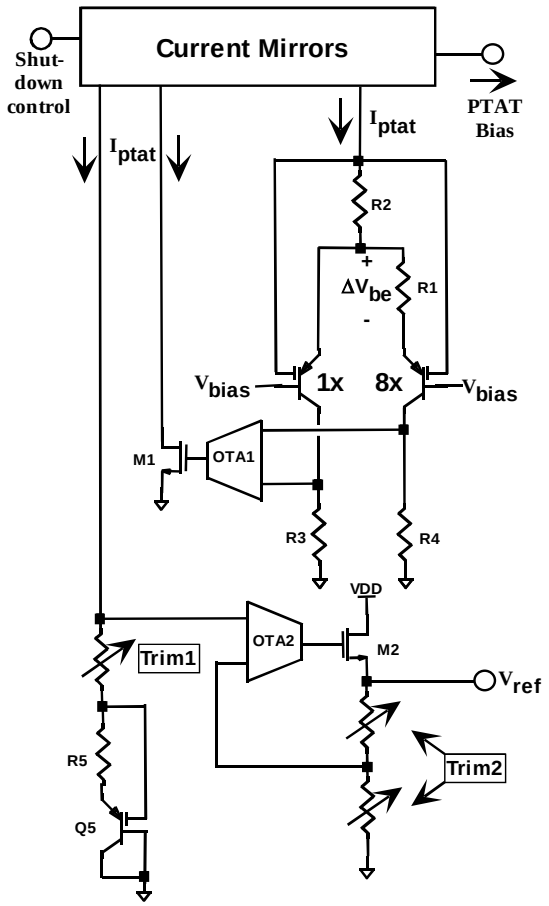

Figure 3: VREF Block Structure

The rest of the task of generating the reference voltage consists in amplifying the PTAT voltage such that when summed with a forward diode drop (lateral PNP Vbe) which has a relatively linear negative temperature coefficient. The result is a temperature invariant voltage.

In the circuit of Figure 3 the ΔVbe amplification is accomplished by the combination of lateral PNP current mirrors and applying PTAT current across resistor R5. The voltage across both R5 and the trim network (Trim1), when summed with the Vbe of transistor Q5 results in a temperature insensitive voltage.

All of the resistors in Figure 3 are implemented as thin-film CrSiN resistors. Trim1 is laser-trimmed to achieve the required low temperature drift. This trimming is done at wafer level test after collecting data at 200°C using a hot-chuck wafer probe.

After trimming to achieve the required temperature stability, another low-noise (large device geometry) OTA is used in connection with a second trim network (Trim2) to trim the output voltage, VREF, to precisely 1.5V. The shut-down control may be used to shut down the circuit by turning off the current mirrors and "starving all of the devices" for current. Not shown are start-up circuitry and resistor-capacitor networks used to insure loop-stability.

The primary outputs of the VREF block are a 1.5V un-buffered reference, and a PTAT current source. The PTAT current source is mirrored with appropriate device geometry scaling to provide the PTAT current source output (I_{temp2}). In fact, the PTAT current is scaled and replicated multiple times in this application for other on-chip functional blocks of the Deep Trek A-to-D converter.

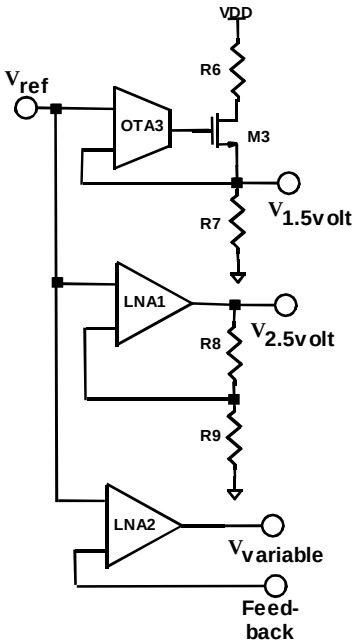

Figure 4: Buffer Block

4.3 Voltage Buffer Block

The buffer block is shown in Figure 4. This block consists of two low-noise amplifiers and a low-noise OTA with an N-channel source-follower output. The LNAs have the same input stage as the OTAs, but additionally have an active push/pull output driver. The reason that the 1.5V output does not use an LNA is that it is required to have a fast-settling output (to drive the sigma-delta A-to-D front end). Adding an output stage requires additional compensation to insure loop stability. Given the very large device geometries employed to manage 1/f noise, it was not possible to compensate an output stage and simultaneously meet the settling requirements of the A-to-D.

4.3 Current Reference Block

The current reference block is shown in Figure 5. This block generates two matched temperature-stable 200 μA current sources, I_{ref1} and I_{ref2}. This is accomplished by the voltage-to-current converter (OTA4, source-follower and resistor) that generates a constant (i.e., temperature-stable) current. This is mirrored by the current mirror network to provide outputs I_{ref1} and I_{ref2} directly. The mirror network can be laser-trimmed if required to precisely scale the output current values.

The Current Reference Block also generates the voltage-mode and current-mode PTRT thermometer outputs, V_{temp} and I_{temp1}. A PTAT voltage is developed across R10 by impressing on it PTAT current from the VREF block. This PTAT voltage is replicated across R11 by OTA5 and feedback from the source-follower output. Part of the PTAT current flowing in resistor R11 is comprised of temperature-stable (i.e., constant) current from the mirror network shown. That being the case, the current flowing in the leg that includes the source-follower after OTA5 is forced by the feedback of OTA5 to be I_{PTAT}-$I_{CONSTANT}$. Subtracting the constant current term introduces an offset in the PTAT current, rendering it PTRT with the reference point established by the trimmed mirror network. A final trim to scale the output may be applied in a second laser-trimmed mirror network.

All of the resistors and trim-networks in this block are made using thin-film CrSiN. This material has a typical temperature coefficient of resistance of -100ppm/°C. The same material is used in the band-gap where I_{ptat} is derived. Therefore I_{ptat} will vary as the CrSiN resistance varies. If I_{ptat} is mirrored or scaled and then applied to another CrSiN resistor (to develop a voltage output as in the case of V_{temp}), the CrSiN variation with temperature drops out. However, in the case of the current-mode outputs, I_{temp1}, I_{temp2}, and I_{temp1}, I_{temp2} the output current varies directly with the CrSiN temperature coefficient.

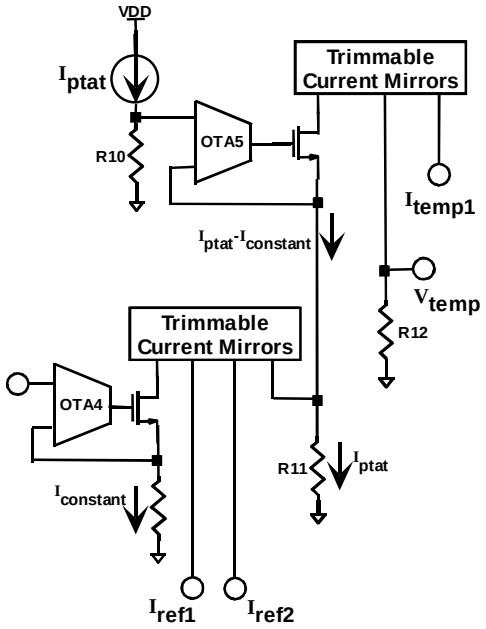

Figure 5: Current Reference Block

5.0 Results

At this time, testing of this block has been limited to wafer-level probe testing mostly un-trimmed die. Additional package-level test results will be presented at the HiTEC conference.

5.1 LNA Results

It has been stressed that low-noise and offset voltage are critical to this application. This is largely dependent on the offset and noise-characteristics resulting from the OTAs and LNAs that are used multiple times. Recall that the noise and offset performance derives from the input pair and load transistor geometries that the OTAs and LNAs have in common.

Thirty-nine LNA die were wafer-probed at room temperature to measure their offset voltage. The average magnitude (absolute value) of the offset voltage was 198μV. Offset mean and standard deviation of the offset voltage are 92μV and 232μV respectively.

Room temperature noise-voltage density results measured on one sample at room temperature are as follows:

1Hz : 360nV/root-Hz.
10Hz: 110nV/root-Hz.
100Hz: 38nV/root-Hz.

The roughly 3x reduction per decade confirms that this follows a 1/f noise characteristic. It cannot be determined from this data what the wide-band noise floor is, other than to predict it is less than 38nV/root-Hz. These results suggest that the LNAs and OTAs are significant in terms of noise contribution, but not solely dominant.

5.2 Buffered VREF Output Results

Voltage reference trims (Trim1 and Trim2) were completed on a handful of die followed by wafer-level probe testing. Results are shown in Figures 6 and 7.

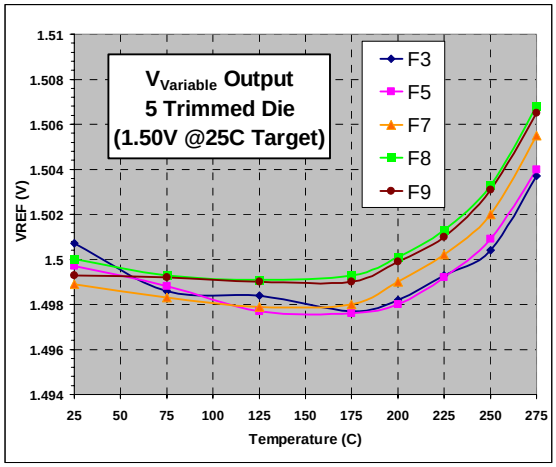

Figure 6: Buffered Reference Output vs. Temperature

Figure 6 shows measurements obtained at the output of the adjustable buffered output ($V_{Variable}$) operated at 1.5V (unity-gain voltage-follower). Results are shown for five die at 25°C intervals from room temperature to 275°C. It can be seen that from 25°C to 225°C the output variation is within 3mV (0.2%) in all cases. Total variation doubles by 275°C, but the reference is clearly still functioning well at this temperature.

Figure 7 shows noise voltage density results at the buffered output ($V_{Variable}$) for 3 die at 25°C and at 225°C. It can be seen that the 1/f noise corner is between 10Hz and 100Hz. From these results total rms output noise in the band from 0.1Hz to 50 Hz can be calculated at about 5µV. This is slightly less than 1 LSB for a 1.5V full-scale signal at 18-bits resolution.

Figures 8 and 9 show the temperature-scaled current outputs. These are for the case of un-trimmed die where the internal reference voltage (VREF) was externally forced to 1.5V. It can be seen that the scale factors and linear output are very close to target.

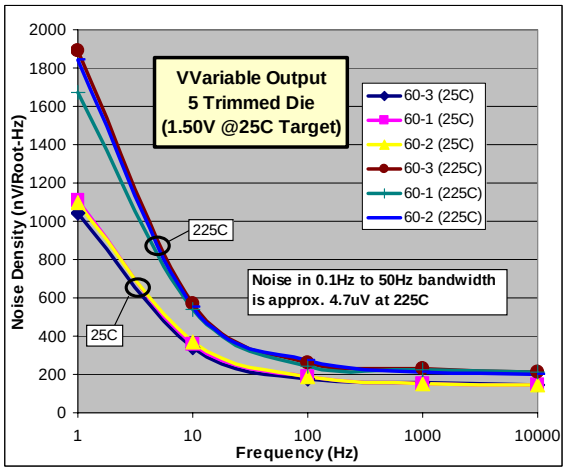

Figure 7: Buffered Reference Output Low-Frequency Noise Characteristics

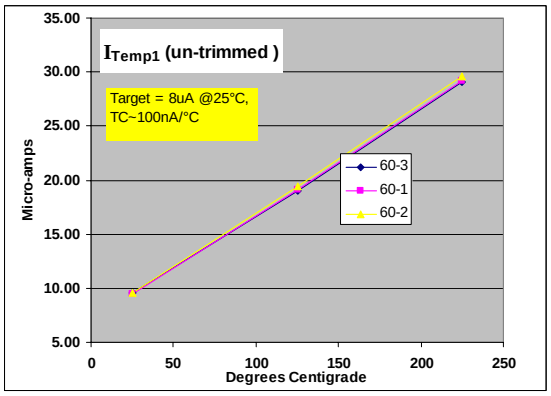

Figure 8: Temperature-scaled Current Source, Itemp1 Output

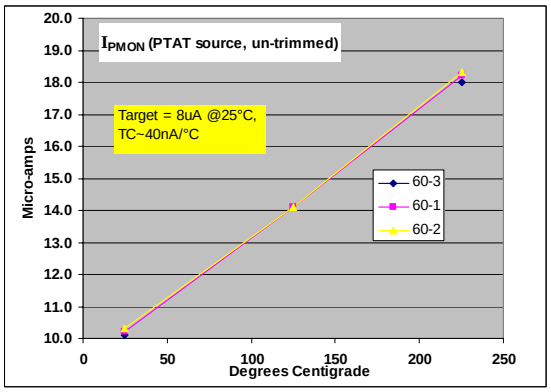

Figure 9: Temperature-scaled Current Source, Itemp2 (PTAT) Output

Wafer-level results were also obtained for the matched constant-current outputs (I_{ref1} and I_{ref2}) up to 225°C. The outputs are within 0.2% of the specified 200uA Worst-case mismatch between the two outputs measured on three die is 0.4%.

6.0 Summary and Conclusions

A general purpose voltage reference and bias block has been realized in SOI CMOS, with demonstrated operation to 275°C. Further testing could extend that result. Very good temperature stability and output noise results have been achieved up to 225°C (0.2% and 5μV rms respectively). Utility reference and thermometer outputs are part of this circuit. This design is meeting all of the performance levels required of the A-to-D converter for which it was developed.

Although this circuit was developed as an embedded block within an A-to-D converter, it could easily be turned into a stand-alone function in a relatively small package (e.g., 14-pin DIP). The test-site implementation reported here is equivalent to about 0.08 inches square (about 2mm x 2mm).

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