REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline U. Add note 2/ to sheet 2. Add note 5/ to table IA. Add note 6/ to t_{WHWL}. Make corrections to notes on sheets 11 and 13. Add note 3 to figure 3. Add note 2 to figure 5, Read Cycle. Add note 6 to figure 5, Write Cycle. Make correction to note 5 of figure 6. Add vendor CAGE 34168 as source of supply for case outline U. Editorial corrections throughout.	97-06-12	Raymond Monnin
B	Corrections to sheet 16, Figure 2, Terminal Connections. - glg	01-01-05	Raymond Monnin
C	Change CAGE code to correct CAGE of 67268. Update boilerplate. Editorial changes throughout. - gap	02-04-08	Raymond Monnin
D	Updated paragraph 4.4.4.2d; added paragraph 4.4.4.2e, and added paragraph 6.6.3. Corrected the S dimension for the Y package and corrected the polarity of the capacitor pads for package Z. Updated boilerplate as part of 5 year review. - ksr	09-05-18	Joseph Rodenbeck
E	Updated body of drawing to reflect current requirements. Added appendix B for die. - glg	11-10-18	Charles F. Saffle
F	Updated Figure 4 to reflect vendor's current modeling and testing methods. Removed class M references. - glg	13-12-20	Charles F. Saffle
G	Add supply voltage ramp time to section 1.4. Updated table IB to reflect vendor's current modeling and testing methods. - glg	14-04-10	Charles F. Saffle
H	Correct Table IA timing parameter Chip enable/select access time (tEHQV/tSLQV) by moving from minimum to maximum column. - glg	14-08-08	Charles F. Saffle
J	Updated drawing to reflect current MIL-PRF-38535 requirements. Correct 1.3 for Supply voltage range and Maximum power dissipation. Update 2.2. Update 4.2.2 to 4.2.1. Correct 4.4.4.2 for time. - llb	14-11-24	Charles F. Saffle
K	Update to current MIL-PRF-38535 requirements. – llb	20-11-09	James Eschmeyer

REV																				
SHEET																				
REV	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	K	K	K	K	K	K	K	K	K	K	K	K	K
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Jeff Bowling

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COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Jeff Bowling

APPROVED BY
Michael. A. Frye

DRAWING APPROVAL DATE
96-11-26

REVISION LEVEL
K

MICROCIRCUIT, MEMORY, DIGITAL, RADIATION-HARDENED, CMOS/SOI, 32K X 8 STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95845**

SHEET 1 OF 34

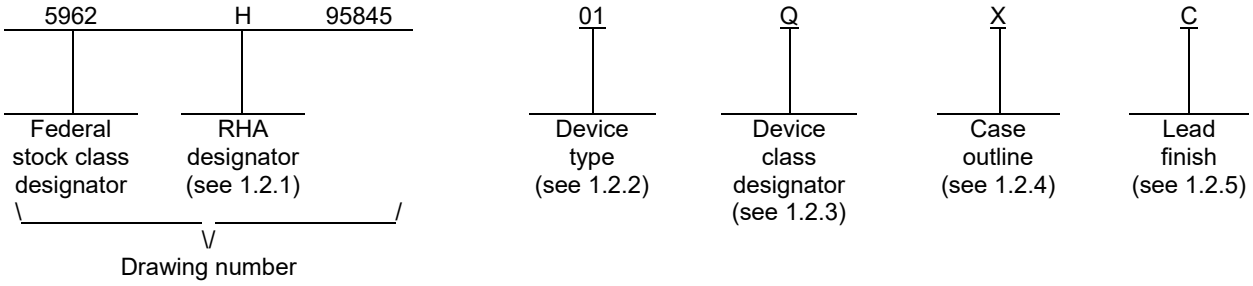
DSCC FORM 2233
APR 97

5962-E060-21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Input/output levels	Chip enable 1/	Access time
01	HX6256	32K X 8 CMOS/SOI SRAM	CMOS	Dual	25 ns
02	HX6256	32K X 8 CMOS/SOI SRAM	TTL	Dual	25 ns
03	HX6356	32K X 8 CMOS/SOI SRAM	CMOS	Dual	25 ns
04	HX6356	32K X 8 CMOS/SOI SRAM	TTL	Dual	25 ns
05	HX6256	32K X 8 CMOS/SOI SRAM	CMOS	Dual	20 ns
06	HX6256	32K X 8 CMOS/SOI SRAM	TTL	Dual	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	See figure 1	28	Flat pack
Z	See figure 1	36	Flat pack
U	See figure 1	36	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Any device type ordered in case outlines X or Y is single chip enable.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+270°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	See MIL-STD-1835
Cases Y, Z, and U	2.0°C/W
Output voltage applied to high Z state	-0.5 V dc to V_{CC} + 0.5 V dc
Maximum power dissipation (P_D)	2.5 W
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc (min) to 5.5 V dc (max)
Supply voltage (V_{SS})	0.0 V dc
Supply voltage ramp time	50 ms maximum
High level input voltage range (V_{IH}):	
Device type 01, 03, 05 (CMOS levels)	0.7 x V_{CC} to V_{CC} + 0.3 V dc
Device type 02, 04, 06 (TTL levels)	2.2 V dc to V_{CC} + 0.3 V dc
Low level input voltage range (V_{IL}):	
Device type 01, 03, 05 (CMOS levels)	-0.3 V dc to 0.3 x V_{CC}
Device type 02, 04, 06 (TTL levels)	-0.3 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	1 Mrads(Si)
Single event phenomenon (SEP) (see 4.4.4.3):	
Heavy ion test:	
No SEL at an effective LET	≤ 120 MeV-cm^2/mg
SEU error rate	1.0 x 10^{-10} upsets/bit-day 4/

1.6 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, method 5012)	100 percent

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltages referenced to V_{SS} (V_{SS} = ground), unless otherwise specified.
4/ Based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield. Weibull parameters are available from the vendor to calculate projected upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix B to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix A. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.2.8 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -5 mA, V_{IL} = 1.35 V, V_{IH} = 3.15 V	1, 2, 3	01, 03, 05	4.2		V
		V_{CC} = 4.5 V, I_{OH} = -4 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V		02, 04, 06	4.2		
		M, D, L, P, R, F, G, H	1 1/		2/		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{IL} = 1.35 V, V_{IH} = 3.15 V	1, 2, 3	01, 03, 05		0.4	V
		V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V		02, 04, 06		0.4	
		M, D, L, P, R, F, G, H	1 1/			2/	
Input leakage current	I_{ILK}	V_{IN} = 0.0 V to 5.5 V, all other pins at 0.0 V, V_{CC} = 5.5 V	1, 2, 3	All	-5	5	µA
		M, D, L, P, R, F, G, H	1 1/		2/	2/	
Output leakage current	I_{OLK}	V_{OUT} = 0.0 V to 5.5 V, all other pins at 0.0 V, V_{CC} = 5.5 V	1, 2, 3	All	-10	10	µA
		M, D, L, P, R, F, G, H	1 1/		2/	2/	
Data retention voltage	V_{DR}	V_{CC} = 2.5 V	1, 2, 3	All	2.5		µA
		M, D, L, P, R, F, G, H	1 1/		2/		
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, no output loading $\overline{S}$ = GND, E = V_{CC} 4/, f = f_{MAX} 3/	1, 2, 3	All		160	mA
		M, D, L, P, R, F, G, H	1 1/			2/	
Supply current (deselected)	I_{CC2}	V_{CC} = 5.5 V, f = f_{MAX} 3/ $\overline{S}$ = V_{CC}, E = GND 4/	1, 2, 3	All		1.5	mA
		M, D, L, P, R, F, G, H	1 1/			2/	
Supply current (standby)	I_{CC3}	V_{CC} = 5.5 V, f = 0 Mhz, $\overline{S}$ = V_{CC}, E = GND	1, 2, 3	All		1.5	mA
		M, D, L, P, R, F, G, H	1 1/			2/	
Data retention current	I_{CC4}	V_{CC} = 2.5 V	1, 2, 3	01, 02, 05, 06		500	µA
		V_{CC} = 3.0 V		03, 04		330	
		M, D, L, P, R, F, G, H	1 1/			2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance 5/	C_{IN}	V_I = 5.0 V or 0.0 V, f = 1 MHz T_A = +25°C, see 4.4.1d	4	All		7	pF
Output capacitance 5/	C_{OUT}	V_O = 5.0 V or 0.0 V, f = 1 MHz T_A = +25°C, see 4.4.1d	4	All		9	pF
Functional tests		See 4.4.1c	7, 8A, 8B	All			
		M, D, L, P, R, F, G, H	7 1/		2/		
Read cycle time	t_{AVAV}	See figures 4 and 5	9, 10, 11	All	25		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Address access time	t_{AVQV}	See figures 4 and 5	9, 10, 11	All		25	ns
		M, D, L, P, R, F, G, H	9 1/			2/	
Chip enable/select access time 4/	t_{EHQV} t_{SLQV}	See figures 4 and 5	9, 10, 11	All		25	ns
		M, D, L, P, R, F, G, H	9 1/			2/	
Output hold after address change	t_{AVQX}	See figures 4 and 5	9, 10, 11	All	3		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Output enable access time	t_{GLQV}	See figures 4 and 5	9, 10, 11	All		9	ns
		M, D, L, P, R, F, G, H	9 1/			2/	
Chip enable/select to output active 4/	t_{EHQX} t_{SLQX}	See figures 4 and 5	9, 10, 11	All	5		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Output enable to output active	t_{GLQX}	See figures 4 and 5	9, 10, 11	All	0		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Chip disable/deselect to output disable 4/	t_{ELQZ} t_{SHQZ}	See figures 4 and 5	9, 10, 11	All		10	ns
		M, D, L, P, R, F, G, H	9 1/			2/	
Output enable to output disable	t_{GHQZ}	See figures 4 and 5	9, 10, 11	All		9	ns
		M, D, L, P, R, F, G, H	9 1/			2/	
Write enable to output disable	t_{WLQZ}	See figures 4 and 5	9, 10, 11	All		9	ns
		M, D, L, P, R, F, G, H	9 1/			2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data setup to end of write	t_{DVWH}	See figures 4 and 5	9, 10, 11	All	15		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Data hold after end of write	t_{WHDX}	See figures 4 and 5	9, 10, 11	All	0		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Output active after end of write	t_{WHQX}	See figures 4 and 5	9, 10, 11	All	5		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Write cycle time 6/ 7/	t_{AVAV}	See figures 4 and 5	9, 10, 11	01 – 04	25		ns
				05, 06	20		
		M, D, L, P, R, F, G, H	9 1/		2/		
Chip enable/select to end of write 4/	t_{EHWH} t_{SLWH}	See figures 4 and 5	9, 10, 11	All	20		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Address setup to end of write	t_{AVWH}	See figures 4 and 5	9, 10, 11	All	20		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Address setup to start of write	t_{AVWL}	See figures 4 and 5	9, 10, 11	All	0		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Write pulse width	t_{WLWH}	See figures 4 and 5	9, 10, 11	All	20		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Address hold after end of write	t_{WHAX}	See figures 4 and 5	9, 10, 11	All	0		ns
		M, D, L, P, R, F, G, H	9 1/		2/		
Write disable pulse width 5/	t_{WHWL}	See figures 4 and 5	9, 10, 11	All	5		ns
		M, D, L, P, R, F, G, H	9 1/		2/ 4/		

1/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$. The M, D, L, P, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.
2/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
3/ $f_{MAX} = 1/t_{AVAV}$ (minimum read cycle time).
4/ Input E and timing parameters t_{EHQV}, t_{EHQX}, t_{ELQZ}, and t_{EHWH} do not apply to devices in case outline X or Y.
5/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.
6/ Outputs disabled.
7/ $t_{AVAV} = t_{WLWH} + t_{WHWL}$.

TABLE IB. SEP test limits. 1/ 2/

Device type	Ion type	Memory pattern	V_{CC} = 4.5 V SEU Rate Adam's 90% worst-case environment 3/	Bias for latch-up test V_{CC} = 5.5 V, no latch-up LET = 4/
All	Heavy Ion	5/	1.0×10^{-10} upsets/bit-day	LET ≤ 120 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.3 herein.

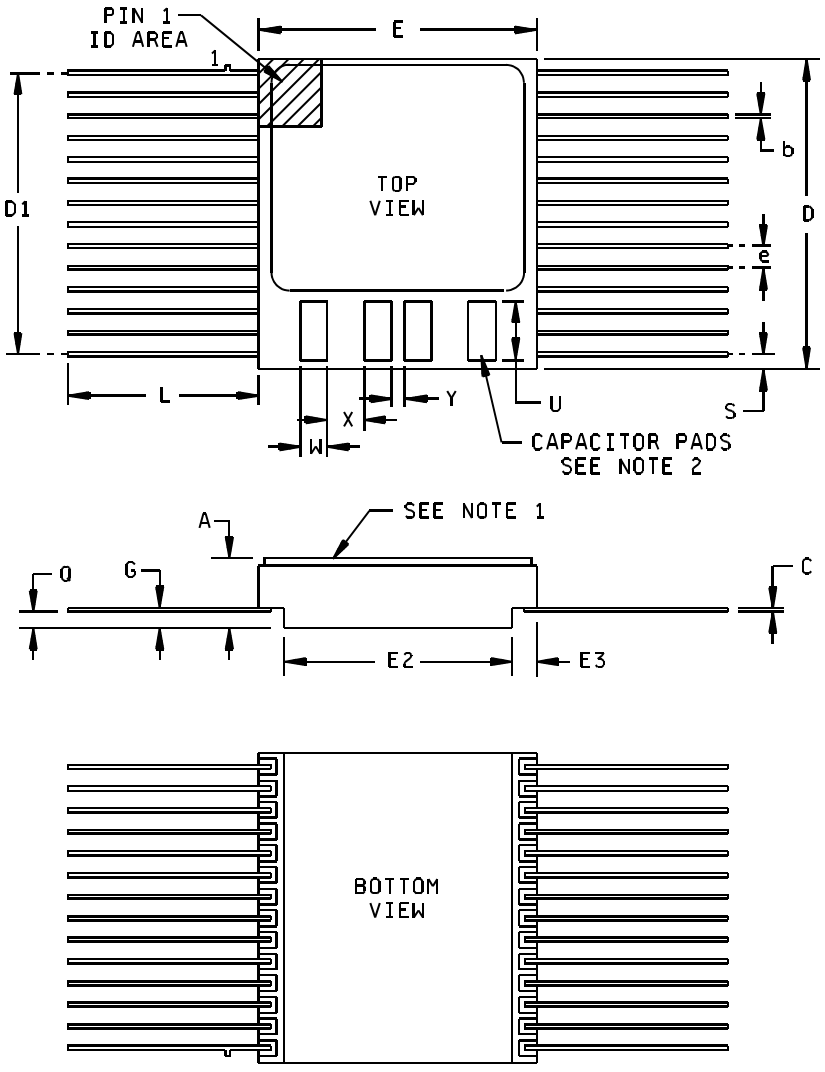
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield. Weibull parameters are available from the vendor to calculate projected upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).

4/ Worst case temperature T_A = +125°C ± 10°C for latch up.

5/ Testing shall be performed using checkerboard and checkerboard bar test patterns.

Case Y



NOTE: The package may be assembled with CDR33 chip capacitors 0.1 µF with 50V rating which meet approved criteria and are similar to MIL-PRF-123 capacitors.

FIGURE 1. Case outlines – Continued.

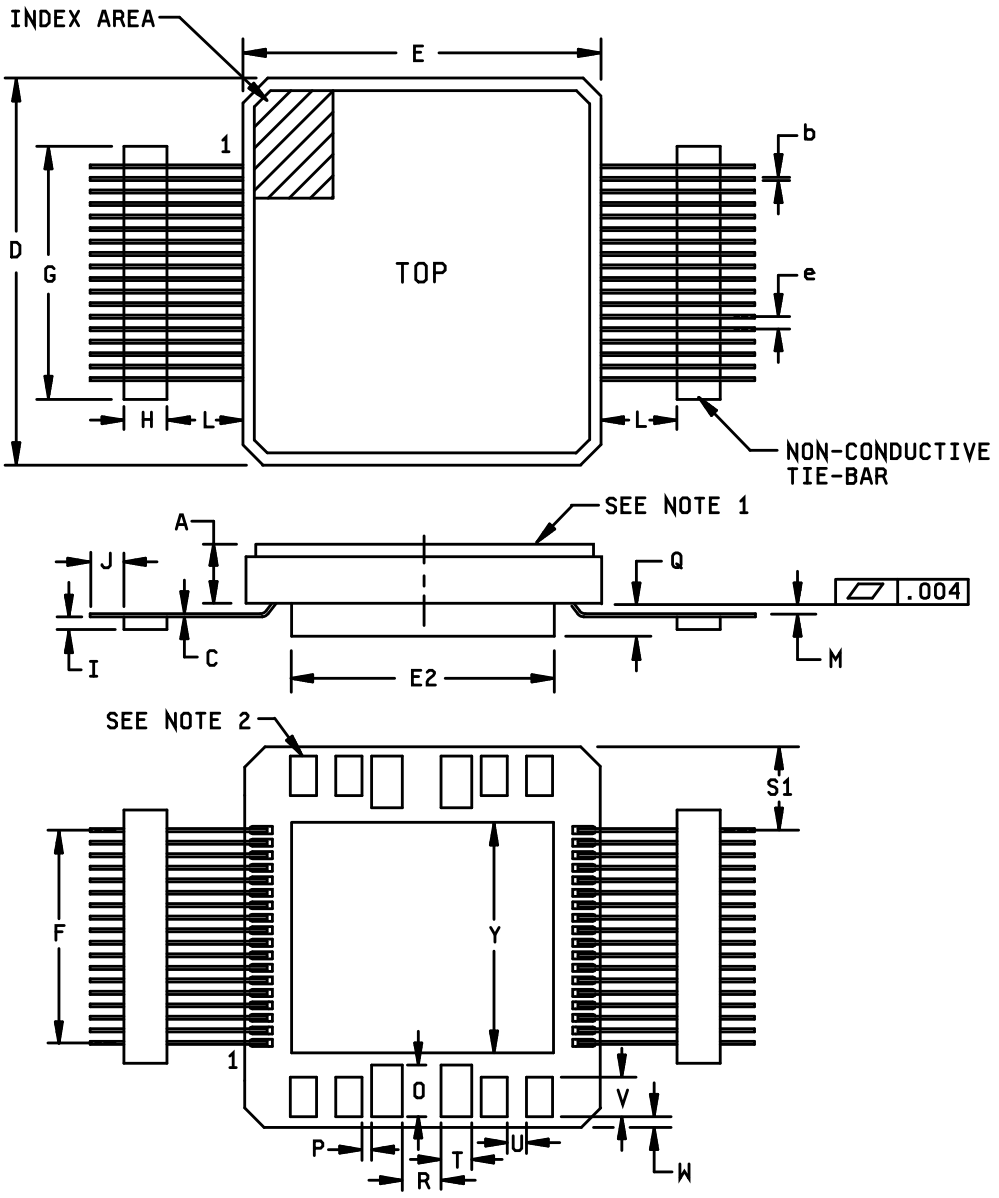
Case Y – Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.29	3.05	.090	.120
b	0.38	0.48	.015	.019
C	0.08	0.15	.003	.006
D	18.08	18.49	.712	.728
D1	16.38	16.64	.645	.655
E	12.52	12.88	.493	.507
E2	9.45	9.86	.372	.388
E3	1.52 REF		.060 BSC	
e	1.27 BSC		.050 BSC	
G	0.79	0.99	.031	.039
L	7.49	---	.295	---
Q	0.66	1.14	.026	.045
S	0.64	1.14	.025	.045
U	3.30 REF		.130 REF	
W	1.27 REF		.050 REF	
X	1.91 REF		.075 REF	
Y	0.25 REF		.010 REF	

NOTES:
1. Lid tied to V_{SS}.
2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (top view) through P4.

FIGURE 1. Case outlines – Continued.

Case Z



NOTE: The package may be assembled with CDR33 0.1 µF and CDR32 .039 µF chip capacitors with 50 V rating which meet approved criteria and are similar to MIL-PRF-123 capacitors.

FIGURE 1. Case outlines.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.16	2.67	.085	.105
b	0.15	0.25	.006	.010
C	0.127	0.191	.0050	.0075
D	16.26	16.76	.640	.660
E	15.85	16.18	.623	.637
E2	11.43 REF		.450 REF	
e	0.635 BSC		.025 BSC	
F	10.67	10.92	.420	.430
G	13.34 REF		.525 REF	
H	3.43 REF		.135 REF	
I	0.64	0.89	.025	.035
J	2.03 REF		.080 REF	
L	6.86	7.62	.270	.300
M	0.13	0.28	.005	.011
O	2.29 REF		.090 REF	
P	0.38 REF		.015 REF	
Q	1.02	1.52	.040	.060
R	1.91 REF		.075 REF	
S1	2.62	3.12	.103	.123
T	1.27 REF		.050 REF	
U	0.76 REF		.030 REF	
V	2.03 REF		.080 REF	
W	0.13 REF		.005 REF	
Y	10.16 REF		.400 REF	

NOTES:
1. Lid tied to V_{SS}.
2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P12.

FIGURE 1. Case outlines - continued.

Case U

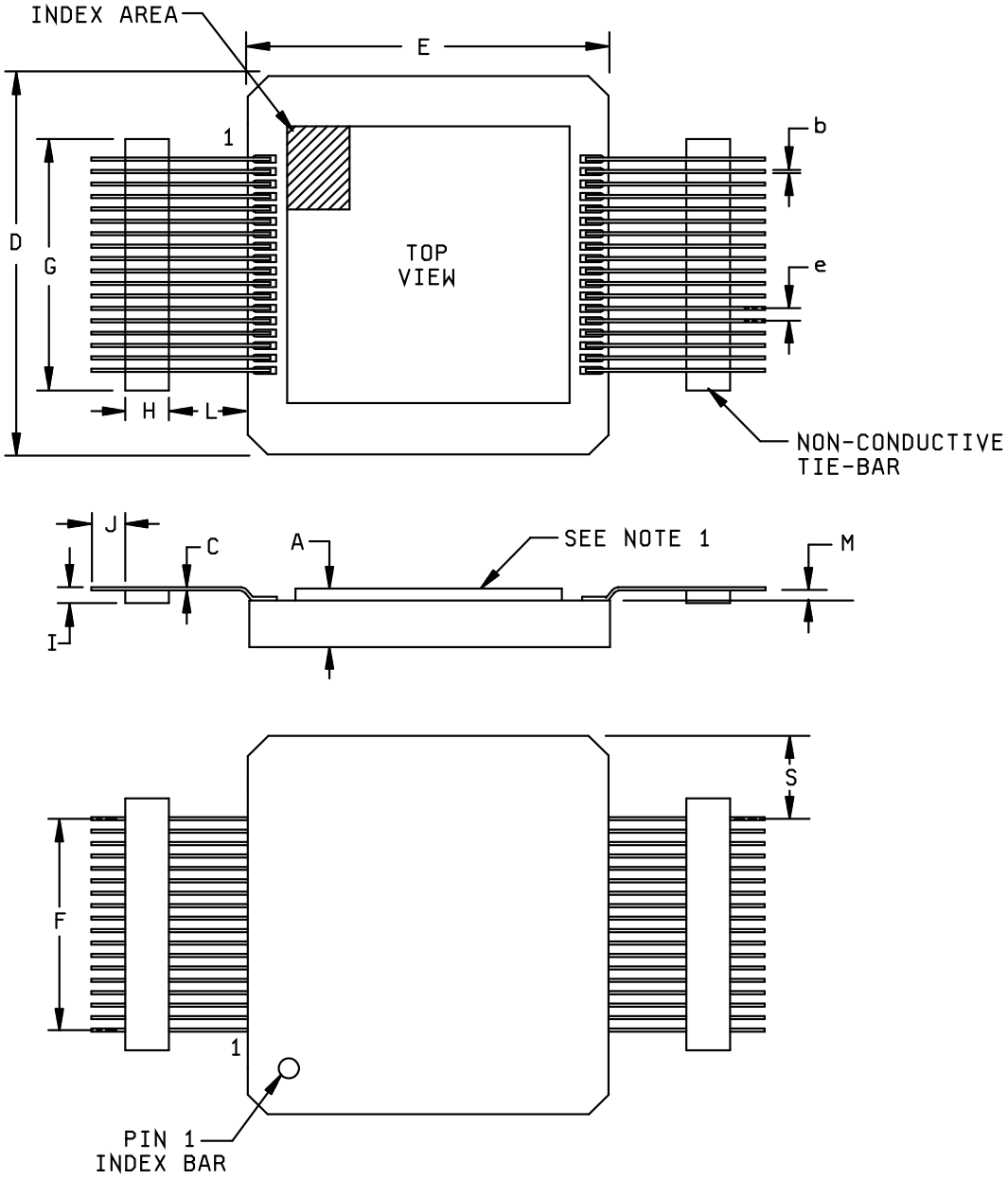


FIGURE 1. Case outlines - continued.

Case U – Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.91	2.41	.075	.095
b	0.15	0.25	.006	.010
C	0.127	0.191	.0050	.0075
D	16.26	16.76	.640	.660
E	15.85	16.18	.623	.637
e See note 2	0.635 BSC		.025 BSC	
F See note 2	10.67	10.92	.420	.430
G	13.34 REF		.525 REF	
H	3.43 REF		.135 REF	
I	0.64	0.89	.025	.035
J	2.03 REF		.080 REF	
L	6.86	7.37	.270	.290
M	0.15	0.30	.006	.012
S	2.62	3.12	.103	.123

NOTES:
1. Lid tied to V_{SS}.
2. Dimensions e and F are measured at the tie bar.

FIGURE 1. Case outlines – Continued.

Device type	All			
Case outline	X	Y	Z	U
Terminal no.	Terminal symbol			
1	A_{14}	A_{14}	GND	GND
2	A_{12}	A_{12}	V_{CC}	V_{CC}
3	A_7	A_7	A_{14}	A_{14}
4	A_6	A_6	A_{12}	A_{12}
5	A_5	A_5	A_7	A_7
6	A_4	A_4	A_6	A_6
7	A_3	A_3	A_5	A_5
8	A_2	A_2	A_4	A_4
9	A_1	A_1	A_3	A_3
10	A_0	A_0	A_2	A_2
11	I/O_0	I/O_0	A_1	A_1
12	I/O_1	I/O_1	A_0	A_0
13	I/O_2	I/O_2	I/O_0	I/O_0
14	GND	GND	I/O_1	I/O_1
15	I/O_3	I/O_3	I/O_2	I/O_2
16	I/O_4	I/O_4	NC	NC
17	I/O_5	I/O_5	V_{CC}	V_{CC}
18	I/O_6	I/O_6	GND	GND
19	I/O_7	I/O_7	GND	GND
20	$\overline{S}$	$\overline{S}$	V_{CC}	V_{CC}
21	A_{10}	A_{10}	I/O_3	I/O_3
22	$\overline{G}$	$\overline{G}$	I/O_4	I/O_4
23	A_{11}	A_{11}	I/O_5	I/O_5
24	A_9	A_9	I/O_6	I/O_6
25	A_8	A_8	I/O_7	I/O_7
26	A_{13}	A_{13}	$\overline{S}$	$\overline{S}$
27	$\overline{W}$	$\overline{W}$	A_{10}	A_{10}
28	V_{CC}	V_{CC}	$\overline{G}$	$\overline{G}$
29	---	---	A_{11}	A_{11}
30	---	---	A_9	A_9
31	---	---	A_8	A_8
32	---	---	A_{13}	A_{13}
33	---	---	$\overline{E}$	$\overline{E}$
34	---	---	$\overline{W}$	$\overline{W}$
35	---	---	V_{CC}	V_{CC}
36	---	---	GND	GND
P1	---	V_{CC}	GND	---
P2	---	GND	V_{CC}	---
P3	---	V_{CC}	V_{CC}	---
P4	---	GND	GND	---
P5	---	---	GND	---
P6	---	---	V_{CC}	---
P7	---	---	V_{CC}	---
P8	---	---	GND	---
P9	---	---	GND	---
P10	---	---	V_{CC}	---
P11	---	---	V_{CC}	---
P12	---	---	GND	---

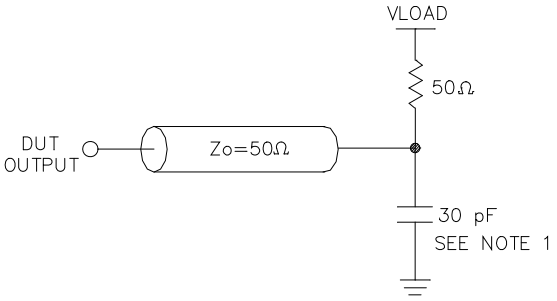
FIGURE 2. Terminal connections.

Mode	Inputs (see notes 1 and 2)					Power
	E (see note 3)	$\overline{S}$	$\overline{W}$	$\overline{G}$	I/O	
Write	High	Low	Low	Don't care	Data in	Active
Read	High	Low	High	Low	Data out	Active
Standby	Don't care	High	Don't care	Don't care	High Z	Standby
Read Standby	High	Low	High	High	High Z	Standby
Standby (see note 4)	Low	Don't care	Don't care	Don't care	High Z	Standby

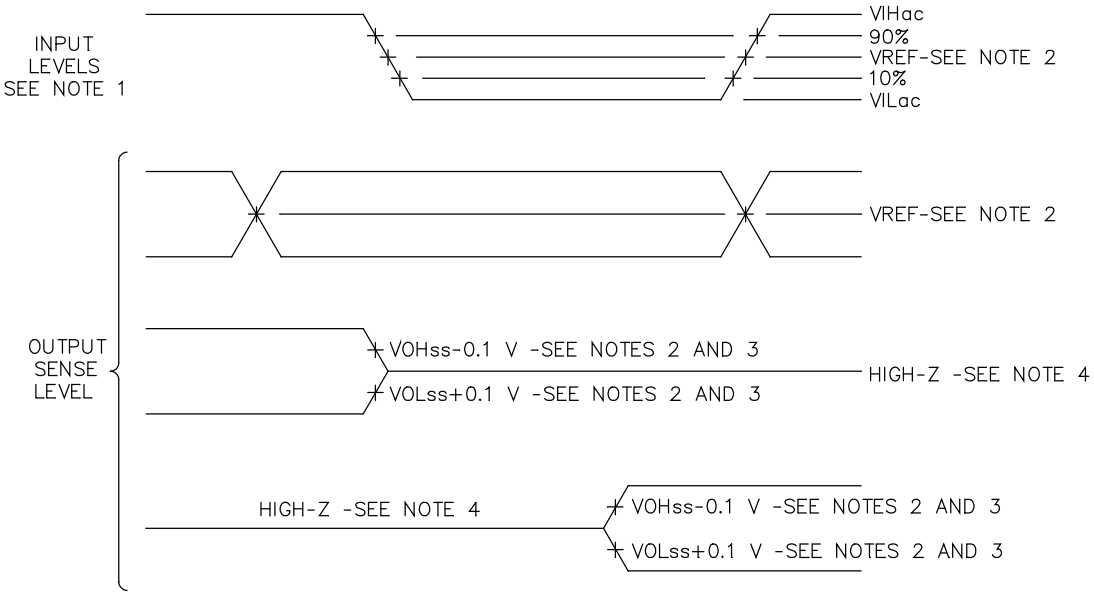
NOTES:
1. V_{IN} for Don't Care inputs = V_{IL} or V_{IH}.
2. When $\overline{G}$ = high, I/O is High-Z.
3. Input E does not apply to devices in case outline X or Y.
4. When in standby mode, $\overline{S}$ = V_{CC} and E = GND input levels to dissipate minimum standby power. All other input levels may float.

FIGURE 3. Truth table.

AC Timing Output Load Circuit



NOTE 1: Set to 5 pF for T*QZ (Low-Z to High-Z) timing parameters.

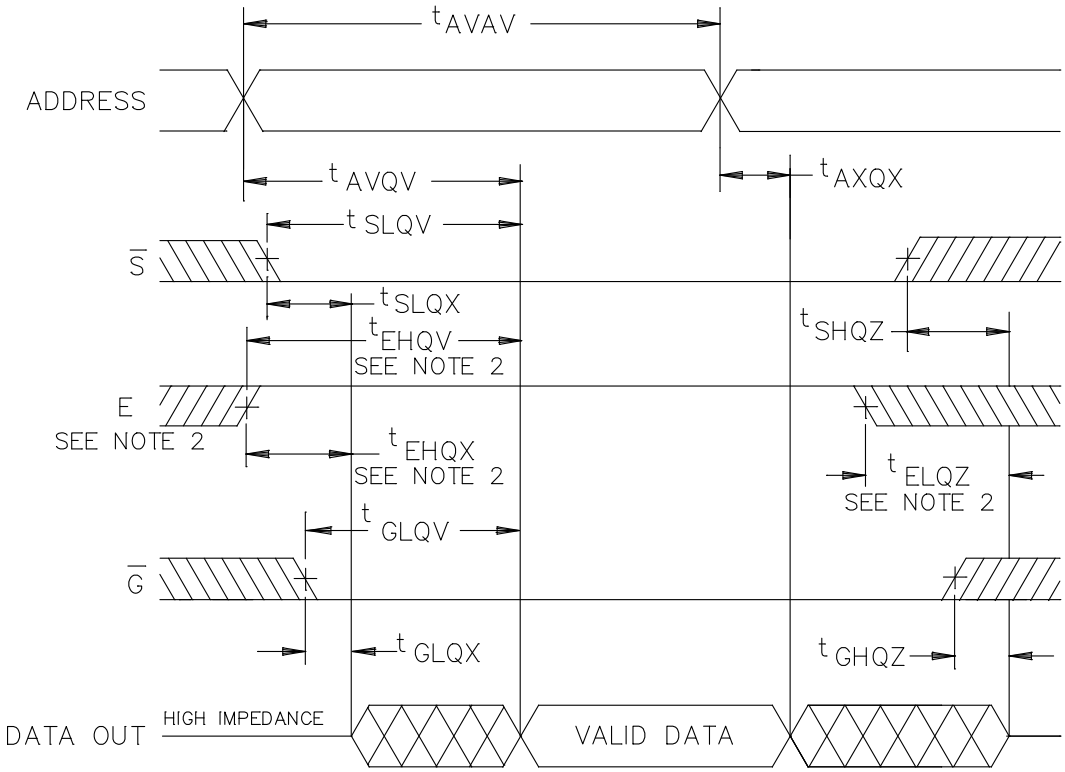


1. All input rise and fall times = 1 ns between the 90% and 10% levels
2. Timing parameter reference voltage level.
3. ss: Low-Z V_{OH} and V_{OL} steady state output voltage.
4. ss: High-Z output pin pulled to V_{Load} by output load circuit.

I/O type	$V_{IH}ac$	$V_{IL}ac$	V_{REF}	V_{LOAD}
5.0 V CMOS	V_{DDIO} – 0.5 V	V_{SS} + 0.5 V	$V_{DDIO}/2$	$V_{DDIO}/2$
5.0 V TTL	3.0 V	0.0 V	1.5 V	1.5 V

FIGURE 4. Output load circuit.

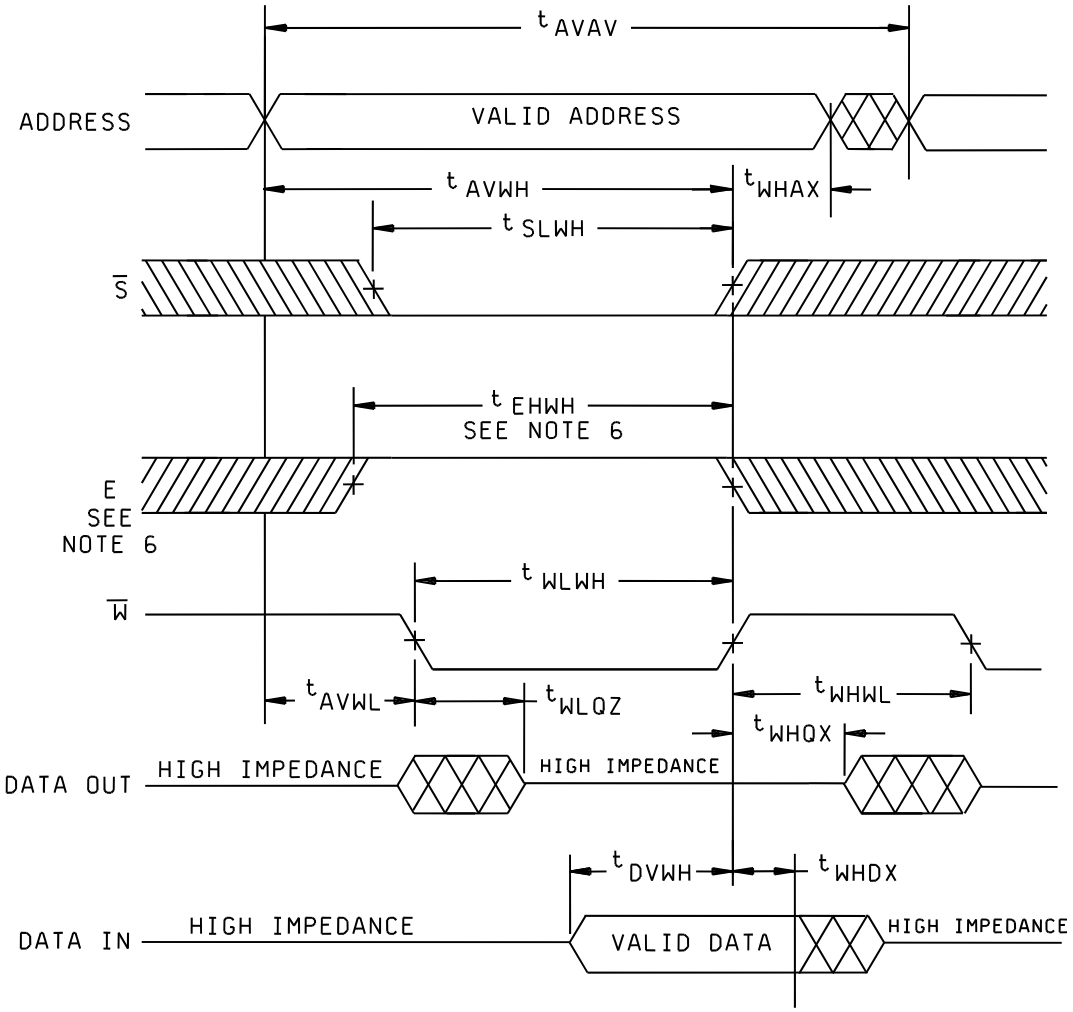
Read cycle (see note 1)



NOTES:
1. $\overline{W}$ is high for read cycle.
2. Input E and timing parameters t_{EHQV}, t_{EHQX}, and t_{ELQZ} do not apply to devices in case outline X or Y.

FIGURE 5. Timing waveforms.

Write cycle (see notes 1, 2, 3, 4, and 5)



NOTES:
1. Write cycle data is latched by the first occurrence of $\overline{S}$ high, E low or $\overline{W}$ high.
2. $\overline{S}$ high, E low, or $\overline{W}$ high must occur while address transitions.
3. Write cycle time is guaranteed for toggling $\overline{S}$ and E or holding $\overline{S}$ or E, or both, in active state.
4. The worst case timing sequence of t_{WLQZ} + t_{DVWH} + t_{WHWL} = the write cycle time (t_{AVAV}).
5. $\overline{G}$ high will eliminate the I/O output from becoming active (t_{WLQZ}).
6. Input E and timing parameter t_{EHWH} do not apply to devices in case outline X or Y.

FIGURE 5. Timing waveforms – Continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1		1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1		1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1d.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device class V performance of delta limits shall be as specified in the manufacturer's QM plan.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC3} standby	±10% of specified value in table IA
I_{ILK}, I_{OLK}	±10% of specified value in table IA

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, method 5012 (see 1.5 herein).

d. O/V (Latch-up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. For device classes Q and V subgroups 1 and 2 of table C-I or table B-I (appendix B) of MIL-PRF-38535, shall be tested as appropriate for device construction.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Transient dose rate upset.

a. For device types 01, 02, 05, and 06, devices shall be capable of retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤ 20 ns up to and including 10^9 Rads (Si)/sec when applied under recommended operating conditions.

b. For device types 03 and 04, devices shall be capable of retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤ 20 ns up to and including 10^9 Rads (Si)/sec when applied under recommended operating conditions.

c. The dose rate upset specification is valid only if the V_{DD} to V_{SS} potential difference applied to the package remains within the recommended operation range during transient radiation.

d. Transient dose rate survivability - Device types 01, 02, 05, 06 shall not be rendered permanently incapable of meeting any functional or electrical specification by a ≤ 20 ns transient ionizing radiation pulse of up to and including 10^{11} Rads (Si)/sec when applied under recommended operating conditions.
The current conducted during the pulse in the SRAM inputs, outputs, and particularly power supply may significantly exceed the normal operating levels.

e. Transient dose rate survivability - Device types 03 and 04 shall not be rendered permanently incapable of meeting any functional or electrical specification by a ≤ 20 ns transient ionizing radiation pulse of up to and including 10^{12} Rads (Si)/sec when applied under recommended operating conditions.
The current conducted during the pulse in the SRAM inputs, outputs, and particularly power supply may significantly exceed the normal operating levels.

4.4.4.3 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the SEC or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature $\pm 10°$C.

f. Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latch-up measurements.

g. For SEP test limits see table IB herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

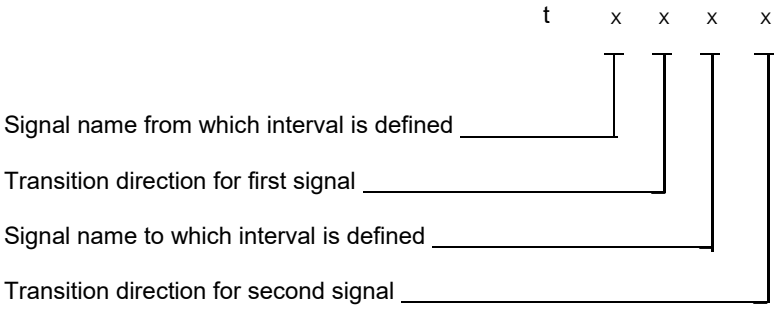
6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. The format is as follows:



a. Signal definitions:

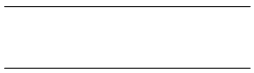
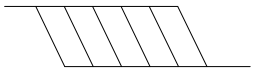
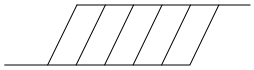
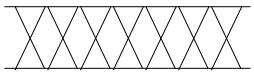
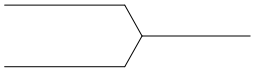
A = Address input bus	S = Chip select
D = Data in	G = Output enable
Q = Data out	E = Chip enable
W = Write enable	

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.2 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.3 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Vendor specific uniquely defining characteristic. This device is similar or identical to other devices available from CAGE code 34168 under different part numbers or SMD numbers. The primary uniquely defining characteristics of this SMD specific part number is contained in paragraphs 4.4.4.2d and e.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latch-up (SEP).

APPENDIX A
Appendix A forms a part of SMD 5962-95845

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

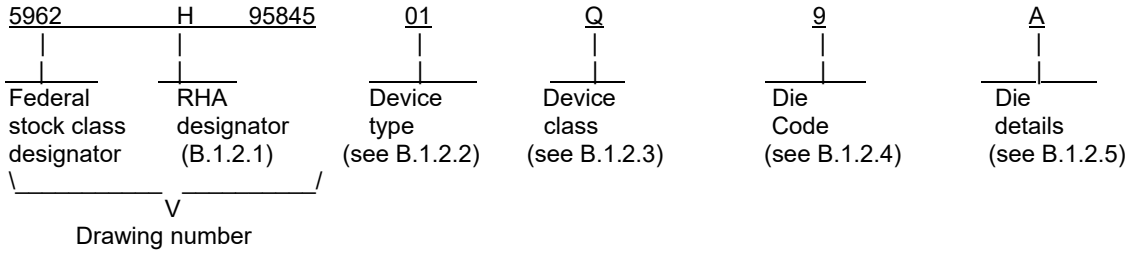
Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

Appendix B
Appendix B forms a part of SMD 5962-95845

B.1 Scope

B.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

B.1.2 PIN. The PIN is as shown in the following example:



B.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

B.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Input/output levels	Chip enable	Access time
01	HX6256	32K X 8 CMOS/SOI SRAM	CMOS	Dual	25 ns
02	HX6256	32K X 8 CMOS/SOI SRAM	TTL	Dual	25 ns
05	HX6256	32K X 8 CMOS/SOI SRAM	CMOS	Dual	20 ns
06	HX6256	32K X 8 CMOS/SOI SRAM	TTL	Dual	20 ns

B.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

B.1.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

B.1.2.5 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

B.1.2.5.1 Die physical dimensions.

Device type	Die size	Die thickness	Die Detail	Figure Number
01	287.7 mils X 277.8 mils	26.6 ± 0.8 mils	A	B-1
02	287.7 mils X 277.8 mils	26.6 ± 0.8 mils	A	B-1
05	287.7 mils X 277.8 mils	26.6 ± 0.8 mils	A	B-1
06	287.7 mils X 277.8 mils	26.6 ± 0.8 mils	A	B-1

B.1.2.5.2 Die bonding pad locations and electrical functions.

Device type	Die Detail	Figure Number
01	A	B-1
02	A	B-1
05	A	B-1
06	A	B-1

B.1.2.5.3 Interface materials.

Device type	Top metalization	Backside metalization	Die Detail	Figure Number
01	Al/Cu, 9kÅ - 11.0 kÅ	Au, 2kÅ	A	B-1
02	Al/Cu, 9kÅ - 11.0 kÅ	Au, 2kÅ	A	B-1
05	Al/Cu, 9kÅ - 11.0 kÅ	Au, 2kÅ	A	B-1
06	Al/Cu, 9kÅ - 11.0 kÅ	Au, 2kÅ	A	B-1

B.1.2.5.4 Assembly related information.

Device type	Glassivation	Die Detail	Figure Number
01	Nitride 9kÅ	A	B-1
02	Nitride 9kÅ	A	B-1
05	Nitride 9kÅ	A	B-1
06	Nitride 9kÅ	A	B-1

B.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

B.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

B.2 APPLICABLE DOCUMENTS.

B.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

B.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3 REQUIREMENTS.

B.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-389535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The Modification in the QM plan shall not effect the form, fit or function as described herein.

B.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

B.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in B.1.2.5.1 and on figure B-1.

B.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in B.1.2.5.2 and on figure B-1.

B.3.2.3 Interface materials. The interface materials for the die shall be as specified in B.1.2.5.3 and on figure B-1.

B.3.2.4 Assembly related information. The assembly related information shall be as specified in B.1.2.5.4 and figure B-1.

B.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

B.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

B.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

B.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

B.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in B.1.2 herein. The certification mark shall be "QML" or "Q" as required by MIL-PRF-38535.

B.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see B.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

B.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

B.4 VERIFICATION

B.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

B.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria within MIL-STD-883, method 5007.
b) 100% wafer probe (see paragraph B.3.4)
c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883, method 2010 or the alternate procedures allowed within MIL-STD-883, method 5004.

B.4.3 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed including groups A, B, C, D and E inspections and as specified herein except where MIL-PRF-38535 permits alternate in-line control testing.

B.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see B.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535.

B.5 DIE CARRIER

B.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

B.6 NOTES

B.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit application (original equipment), design applications, and logistics purposes.

B.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0591.

B.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-HDBK-1331.

B.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see B.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

Pad List	Bond Locations (µm)		Side (East (E), (West (W))	Signal Name
	X location	Y location		
01	-3559.050	3041.150	W	GND
02	-3559.050	2900.150	W	$\overline{G}$
03	-3559.050	2535.800	W	A11
04	-3559.050	2090.800	W	A10
05	-3559.050	1645.800	W	A9
06	-3559.050	1200.800	W	A8
07	-3559.050	755.800	W	GND
08	-3559.050	614.800	W	CMOS/TTL 1/
09	-3559.050	434.500	W	$\overline{W}$
10	-3559.050	-97.150	W	CMOS/TTL 1/
11	-3559.050	-305.150	W	VCC
12	-3559.050	-810.400	W	A7
13	-3559.050	-1255.400	W	A6
14	-3559.050	-1700.400	W	A5
15	-3559.050	-2145.400	W	A4
16	-3559.050	-2590.400	W	A14
17	-3559.050	-3035.400	W	A13
18	-3559.050	-3480.400	W	A12
19	-3559.050	-3621.400	W	GND
20	3443.950	-3613.100	E	GND
21	3443.950	-3472.100	E	A0
22	3443.950	-3027.100	E	A1
23	3443.950	-2582.100	E	A2
24	3443.950	-2124.250	E	D0
25	3443.950	-1692.550	E	D1
26	3443.950	-1260.450	E	D2
27	3443.950	-776.400	E	GND
28	3443.950	-348.750	E	D3
29	3443.950	82.900	E	D4

FIGURE B-1. Bond Pad Locations and Functions.

Pad List	Bond Locations (µm)		Side (East (E), West (W))	Signal Name
	X location	Y location		
30	3443.950	514.600	E	D5
31	3443.950	946.300	E	D6
32	3443.950	1376.300	E	D7
33	3443.950	1807.750	E	$\overline{S}$
34	3443.950	2252.750	E	A3
35	3443.950	2617.100	E	E
36	3443.950	2825.100	E	VCC
37	3443.950	3033.100	E	GND

1/ The two CMOS/TTL pins on the 256K die must be wire-bonded either to the VDD or GND plane in the package. For CMOS input configuration, bond both CMOS pads to VDD, for TTL input configuration, bond both CMOS pads to GND. **The pads must not be left floating**.

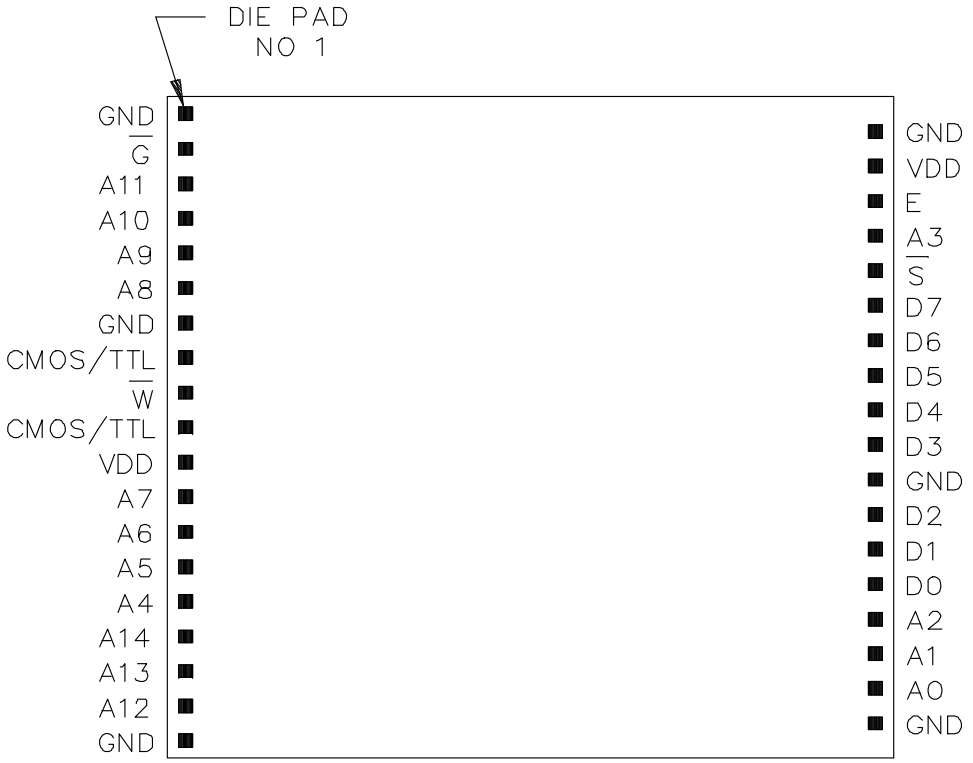


FIGURE B-1. Bond Pad Locations and Functions – Continued.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 20-11-06

Approved sources of supply for SMD 5962-95845 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9584501QXC	34168	HX6256/RQFC
5962F9584501QYC	34168	HX6256/NQFC
5962F9584501QZC	34168	HX6256/XQFC
5962F9584501VXC	34168	HX6256/RVFC
5962F9584501VYC	34168	HX6256/NVFC
5962F9584501VZC	34168	HX6256/XVFC
5962F9584502QUC	34168	HX6256/PQFT
5962F9584502QXC	34168	HX6256/RQFT
5962F9584502QYC	34168	HX6256/NQFT
5962F9584502QZC	34168	HX6256/XQFT
5962F9584502VUC	34168	HX6256/PVFT
5962F9584502VXC	34168	HX6256/RVFT
5962F9584502VYC	34168	HX6256/NVFT
5962F9584502VZC	34168	HX6256/XVFT
5962F9584503QZC	34168	HX6356/XQFC
5962F9584503VZC	34168	HX6356/XVFC
5962F9584504QUC	34168	HX6356/PQFT
5962F9584504QZC	3/	HX6356/XQFT
5962F9584504VUC	34168	HX6356/PVFT
5962F9584504VZC	3/	HX6356/XVFT
5962F9584505QXC	3/	HX6256/RQFC20
5962F9584505QYC	3/	HX6256/NQFC20
5962F9584505QZC	3/	HX6256/XQFC20
5962F9584505VXC	3/	HX6256/RVFC20
5962F9584505VYC	3/	HX6256/NVFC20
5962F9584505VZC	3/	HX6256/XVFC20
5962F9584506QXC	3/	HX6256/RQFT20
5962F9584506QYC	3/	HX6256/NQFT20
5962F9584506QZC	3/	HX6256/XQFT20
5962F9584506VXC	3/	HX6256/RVFT20

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9584506VYC	3/	HX6256/NVFT20
5962F9584506VZC	3/	HX6256/XVFT20
5962H9584501Q9A	34168	HX6256DIE
5962H9584501QXC	34168	HX6256/RQHC
5962H9584501QYC	34168	HX6256/NQHC
5962H9584501QZC	34168	HX6256/XQHC
5962H9584501VXC	34168	HX6256/RVHC
5962H9584501VYC	34168	HX6256/NVHC
5962H9584501VZC	34168	HX6256/XVHC
5962H9584502Q9A	34168	HX6256DIE
5962H9584502QUC	34168	HX6256/PQHT
5962H9584502QXC	34168	HX6256/RQHT
5962H9584502QYC	34168	HX6256/NQHT
5962H9584502QZC	34168	HX6256/XQHT
5962H9584502VUC	34168	HX6256/PVHT
5962H9584502VXC	34168	HX6256/RVHT
5962H9584502VYC	34168	HX6256/NVHT
5962H9584502VZC	34168	HX6256/XVHT
5962H9584503QZC	34168	HX6356/XQHC
5962H9584503VZC	34168	HX6356/XVHC
5962H9584504QUC	34168	HX6356/PQHT
5962H9584504QZC	3/	HX6356/XQHT
5962H9584504VUC	34168	HX6356/PVHT
5962H9584504VZC	3/	HX6356/XVHT
5962H9584505Q9A	3/	HX6256DIE
5962H9584505QXC	3/	HX6256/RQHC20
5962H9584505QYC	3/	HX6256/NQHC20
5962H9584505QZC	3/	HX6256/XQHC20
5962H9584505VXC	3/	HX6256/RVHC20
5962H9584505VYC	3/	HX6256/NVHC20

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9584505VZC	3/	HX6256/XVHC20
5962H9584506Q9A	3/	HX6256DIE
5962H9584506QXC	3/	HX6256/RQHT20
5962H9584506QYC	3/	HX6256/NQHT20
5962H9584506QZC	3/	HX6256/XQHT20
5962H9584506VXC	3/	HX6256/RVHT20
5962H9584506VYC	3/	HX6256/NVHT20
5962H9584506VZC	3/	HX6256/XVHT20
5962R9584501QXC	34168	HX6256/RQRC
5962R9584501QYC	34168	HX6256/NQRC
5962R9584501QZC	34168	HX6256/XQRC
5962R9584501VXC	34168	HX6256/RVRC
5962R9584501VYC	34168	HX6256/NVRC
5962R9584501VZC	34168	HX6256/XVRC
5962R9584502QUC	34168	HX6256/PQRT
5962R9584502QXC	34168	HX6256/RQRT
5962R9584502QYC	34168	HX6256/NQRT
5962R9584502QZC	34168	HX6256/XQRT
5962R9584502VUC	34168	HX6256/PVRT
5962R9584502VXC	34168	HX6256/RVRT
5962R9584502VYC	34168	HX6256/NVRT
5962R9584502VZC	34168	HX6256/XVRT
5962R9584503QZC	34168	HX6356/XQRC
5962R9584503VZC	34168	HX6356/XVRC
5962R9584504QUC	34168	HX6356/PQRT
5962R9584504QZC	3/	HX6356/XQRT
5962R9584504VUC	34168	HX6356/PVRT
5962R9584504VZC	3/	HX6356/XVRT
5962R9584505QXC	3/	HX6256/RQRC20
5962R9584505QYC	3/	HX6256/NQRC20
5962R9584505QZC	3/	HX6256/XQRC20
5962R9584505VXC	3/	HX6256/RVRC20
5962R9584505VYC	3/	HX6256/NVRC20
5962R9584505VZC	3/	HX6256/XVRC20

See footnotes at end of list.

DATE: 14-11-24

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9584506QXC	3/	HX6256/RQRT20
5962R9584506QYC	3/	HX6256/NQRT20
5962R9584506QZC	3/	HX6256/XQRT20
5962R9584506VXC	3/	HX6256/RVRT20
5962R9584506VYC	3/	HX6256/NVRT20
5962R9584506VZC	3/	HX6256/XVRT20

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34168	Honeywell Aerospace 12001 State Highway 55 Plymouth, MN 55441