

HX422R

Quad RS422 Differential Line Receiver
Radiation Hardened 3.3V SOI CMOS

Features

- Four Independent Receivers
- Rad Hard: 300k Rad(Si) Total Dose
- Single +3.3 V Analog Supply
- Common Receiver Enable Control
- Three-state Outputs
- Temperature Range: -55°C to 125°C
- Built in Hysteresis
- 10mA Output Drive
- Maximum Data Rate: 20Mb/s

Mixed Signal Rad Hard Process

The HX422R is fabricated on space qualified SOI CMOS process. High-speed precision analog circuits are now combined with high-density logic circuits that can reliably withstand the harshest environments.

Low Power

The HX422R dissipates less than 200mW typically with all outputs toggling at 10Mb/s data rate.

Common Receiver Enable Control (EN, EN*)

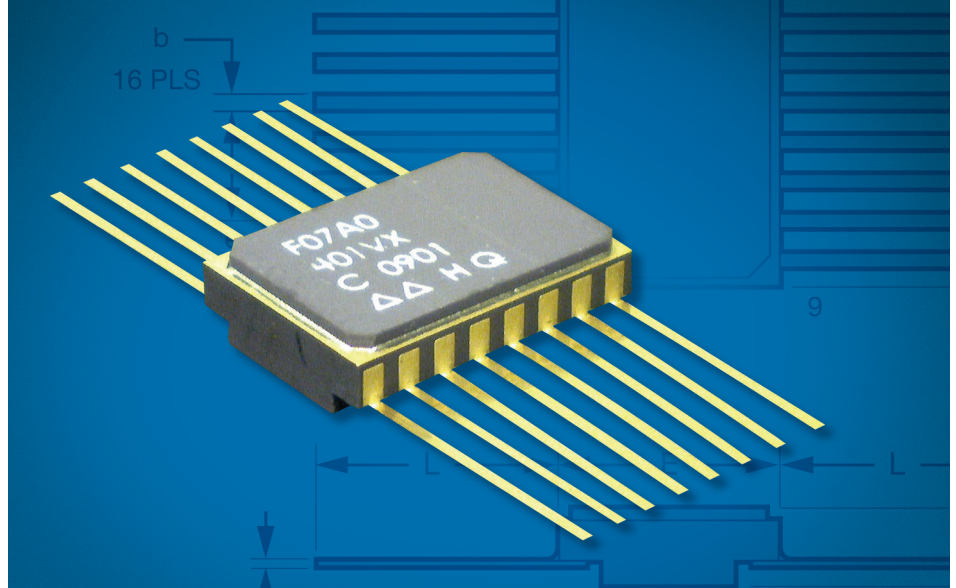
The EN and EN* inputs allow the user to put the digital outputs into high impedance three-state mode.

Dual Power Supply Capability

The HX422R uses a single +3.3V power supply simplifying system power supply design.

Space Qualified Package

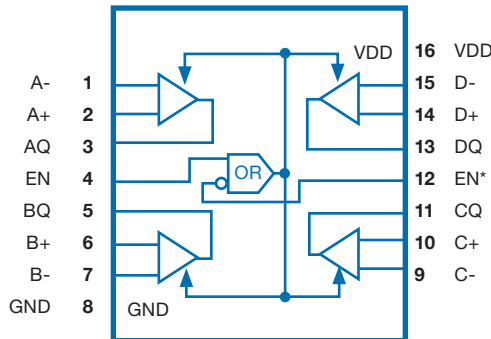
The HX422R is packaged in a 16 lead ceramic flat pack.



The HX422R is a radiation hardened Silicon On Insulator (SOI) CMOS quad differential line receiver designed to meet the standard RS422 requirements and digital data transmission over balanced lines. It features four independent receivers with a common receiver enable

control and high impedance outputs. The HX422R has a maximum operating frequency of 20Mb/s. The circuit has built in hysteresis to improve noise margin and output stability for slow changing input signals.

Package Pinout



Truth Table

EN	EN*	V _{IN(DIFF)}	Q
L	H	X	Z
H	X	<-200 mV	L
X	L	<-200 mV	L
H	X	>+200 mV	H
X	L	>+200 mV	H

Signal Definition

Signal	Description
A+, A- B+, B-	Differential Data Input signals
C+, C- D+, D-	Differential Data Input signals
AQ, BQ, CQ, DQ	Output signals, CMOS levels
EN, EN*	Output Enable Control pins. The combination of EN = L and EN* = H will put the outputs into the high impedance state. All other combinations of EN and EN* will allow data through the drivers.

Recommended Operating Conditions (1)(2)

Parameter	Symbol	Limits		Units
		Min	Max	
Supply Voltage	V_{DD}	3.0	3.6	V
Input Voltage A+/-, B+/-, C+/-, D+/-	$V_{IN(Diff)}$	-7	7	V
Input Voltage (E+, E-)	$V_{IN(Enable)}$	0	VDD	V
Input Common Mode Range A+/-, B+/-, C+/-, D+/-	VCM	-6	+6	V
Differential Input Voltage	V_{DIFF}	-5	+5	V
Output Voltage	VO	-0.3	VDD + 0.3	V
Case Operating Temperature	T_C	-55	+125	°C

(1) Specifications listed in datasheet apply when used under the Recommended Operating Conditions unless otherwise specified.

(2) It is recommended that all unused inputs be held at VDD or ground.

Absolute Maximum Ratings (1)(2)

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
Supply Voltage	V_{DD}	—	-0.5	+6.5	V
DC Input Voltage (EN, EN*)	V_{IN}	—	-0.5	VDD + 0.5	V
Common Mode Range	V_{CM}	—	-7	+7	V
Input Voltage A+/-, B+/-, C+/-, D+/-	$V_{IN(DIFF)}$	—	-8	+8	V
Differential Input Voltage	V_{DIFF}	—	-6.5	+6.5	V
Receiver Output Voltage (AQ, BQ, CQ, DQ)	VO	—	-0.5	VDD + 0.5	V
Input Diode Clamp Current	I_{IK}	—	-180	+180	mA
Output Short Circuit Current (2)	I_{OS}	1 second, 1 output	15	120	mA
Receiver Output Current	I_O	—	-20	+20	mA
Storage Temperature	T_{STO}	—	-65	+150	°C
Thermal Resistance, Junction to Case	θ_{JC}	—	—	16.5	°C/W
Junction Temperature	T_J	—	—	+175	°C
Lead Temperature (soldering, 5 seconds)	T_{LMAX}	—	—	+300	°C
ESD (Human Body Model)	—	—	—	2000	V

(1) Stresses above absolute maximum ratings may cause damage to the device.

(2) Short one output at a time to VSS and do not exceed the maximum junction temperature. The max test time is 1 second.

Radiation Hardness Ratings (1)

Parameter	Symbol	Environment Conditions	Limits	Units
Total Dose	TID	—	300	krad(Si)
Transient Dose Rate Upset	DRU	Pulse width \leq 20ns	1×10^9	rad(Si)/s
Dose Rate Survivability	DRS	Pulse width \leq 20ns	1×10^{12}	rad(Si)/s
Neutron Fluence	—	1MeV equivalent energy	1×10^{14}	N/cm ²

(1) Device will not latch up due to any of the specified radiation exposure conditions.

Radiation Characteristics

Total Ionizing Dose Radiation

The device radiation hardness assurance TID level was qualified by ⁶⁰Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Transient Dose Rate Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. The device will maintain basic functional operation during exposure to a pulse up to the DRU specification. The device will meet functional, timing and parametric specifications after exposure to a pulse up to the DRS specification.

Neutron Irradiation Damage

SOI CMOS is inherently tolerant to damage from neutron irradiation. The device meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup

The device will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

Electrical Requirements (1)(2)(3)

Parameter	Symbols	Conditions	Min	Limits Max	Units
Supply Current		$V_{DD} = 3.6\text{ V}$, all outputs toggling			mA
	I_{DDOP1}	2Mb/s, (CL=85pF for reference)	—	40	
	I_{DDOP3}	10 Mb/s, (CL=85pF for reference)	—	60	
Differential Line Input Voltage (2)	V_{TH6}	$V_{CM} = +6\text{V}$, $V_{DD}=3.0\text{V}$	-200	200	mV
	V_{TH0}	$V_{CM} = 0\text{V}$, $V_{DD}=3.0\text{V}$	-200	200	
	V_{THM6}	$V_{CM} = -6\text{V}$, $V_{DD}=3.0\text{V}$	-200	200	
Differential Line Input Threshold Hysteresis (2) (4)	V_{HY}	$V_{CM} = 0$	5	100	mV
Input Resistance (Line pins) (2) (4)	R_{IN6}	$V_{CM} = +6\text{V}$	6k	15k	Ohms
	R_{IN0}	$V_{CM} = 0$	6k	15k	
	R_{INM6}	$V_{CM} = -6\text{V}$	6k	15k	
Input Current (Line pins) (2)	I_{IH1}	$V_{CM} = +6\text{V}$	—	1000	μA
	I_{IL1}	$V_{CM} = -6\text{V}$	-1300	—	
Input Threshold (E+, E-) (3)	V_{IL}	$V_{DD} = 3.0\text{ V}$	—	0.9	V
Input Threshold (E+, E-) (3)	V_{IH}	$V_{DD} = 3.6\text{ V}$	2.52	—	V
Input Current (Enable) (3)	I_{IH2}	$V_{DD} = 3.6\text{ V}$, $V_{IN} = 3.6\text{V}$	-10	10	μA
	I_{IL2}	$V_{DD} = 3.6\text{ V}$, $V_{IN} = 0\text{V}$	-10	10	
Output Three-state Current	I_{OZL}	$V_{DD} = 3.6\text{ V}$, outputs disabled	-10	10	μA
	I_{OZH}	$V_{DD} = 3.6\text{ V}$, outputs disabled	-10	10	
Output High Voltage	V_{OH}	$I_{OH} = -10\text{ mA}$, $V_{DD} = 3.0\text{V}$	2.5	—	V
Output Low Voltage	V_{OL}	$I_{OL} = 10\text{ mA}$, $V_{DD} = 3.0\text{ V}$	—	0.5	
Input Capacitance Diff Inputs (2) (4)	C_I			12	pF
Output Capacitance CMOS Outputs (4)	C_O			15	pF

(1) Not used.

(2) Differential inputs refer to A-, A+, B-, B+, C-, C+, D-, D+.

(3) E+, E- are the Enable pins.

(4) Guaranteed but not tested.

Timing Parameters (1)

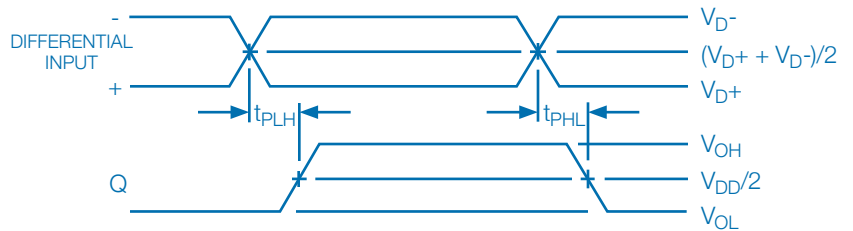
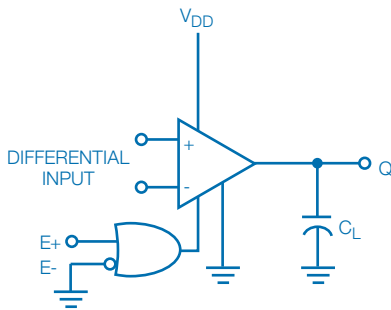
Parameter	Symbol	Condition	Limits		Units
			Min	Max	
Differential Propagation Delay High to Low	T_{PHL1}	$V_{DD} = 3.0, 3.6\text{ V}$ $CL = 15\text{ pF}$ $VDIFF = 500\text{ mV}$	0	54	nS
	T_{PHL2}	$VDIFF = 1000\text{ mV}$	0	45	nS
Differential Propagation Delay Low to High	T_{PLH1}	$V_{DD} = 3.0, 3.6\text{ V}$ $CL = 15\text{ pF}$ $VDIFF = 500\text{ mV}$	0	54	nS
	T_{PLH2}	$VDIFF = 1000\text{ mV}$	0	45	nS
Disable Time High to Z	T_{PHZ}		0	25	nS
Disable Time Low to Z	T_{PLZ}		0	25	nS
Enable Time Z to Low	T_{PZL}		2.5	25	nS
Enable Time Z to High	T_{PZH}		2.5	25	n
Data Rate		$V_{DD} = 3.0, 3.6\text{ V}$			
	F_{DATA1}	$VDIFF = 200\text{ mV}$		10	Mb/s
	F_{DATA2}	$VDIFF = 1000\text{ mV}$		20	Mb/s
Operating Frequency (Clock)		$V_{DD} = 3.0, 3.6\text{ V}$			
	F_{MAX1}	$VDIFF = 200\text{ mV}$		5	MHz
	F_{MAX2}	$VDIFF = 1000\text{ mV}$		10	MHz

(1) The common mode voltage is 1.5V.

Reference Circuits and Timing Diagrams

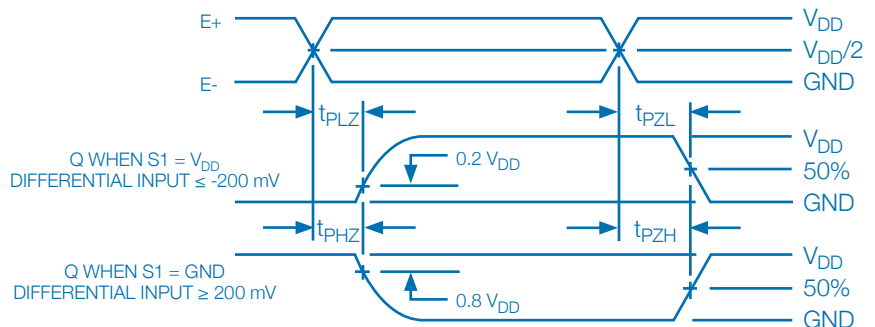
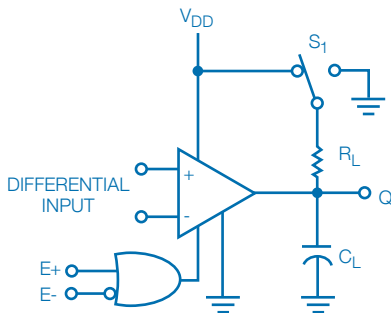
T_{PLH} and T_{PHL} Reference Circuit and Timing Diagram

Circuits and diagrams for reference only. Input edge rate $\leq 5\text{ ns}$.



T_{PHZ} , T_{PZH} , T_{PLZ} , and T_{PZL} Reference Circuit and Timing Diagram

Circuits and diagrams for reference only. Input edge rate $\leq 5\text{ ns}$.



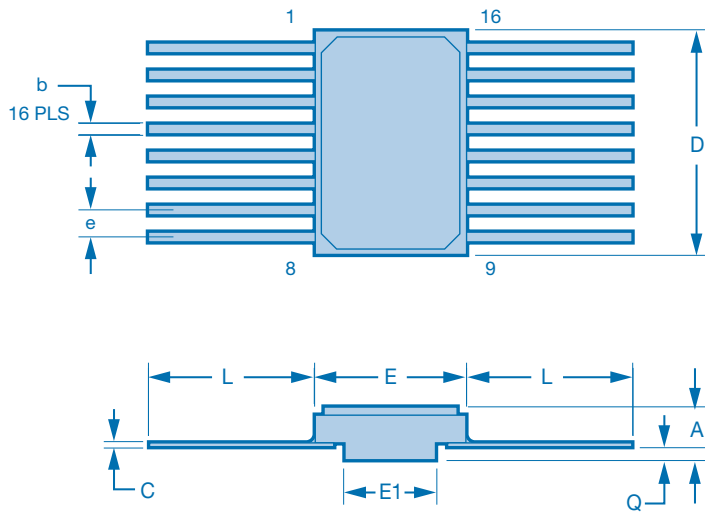
Signal Integrity

As a general design practice, for digital input signals, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of $\leq 10\text{ ns}$. More specifically, an input is considered to have good signal

integrity when the input voltage monotonically traverses the region between V_{IL} and V_{IH} in $\leq 10\text{ ns}$.

Floating inputs for an extended period of time is not recommended.

Package Outline Dimensions



Symbol	Dimensions - Inches		Dimensions - Millimeters	
	Min	Max	Min	Max
A	.101	.125	2.57	3.18
b	.015	.019	0.38	0.48
c	.004	.007	0.11	0.18
D	.392	.408	9.96	10.36
e	.047	.053	1.20	1.34
E	.274	.286	6.96	7.26
E1	.185	.196	4.70	4.96
L	.320	.360	8.13	9.14
Q	.022	.032	0.56	0.82

Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since the early 1990's. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

Screening and Conformance Inspection

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

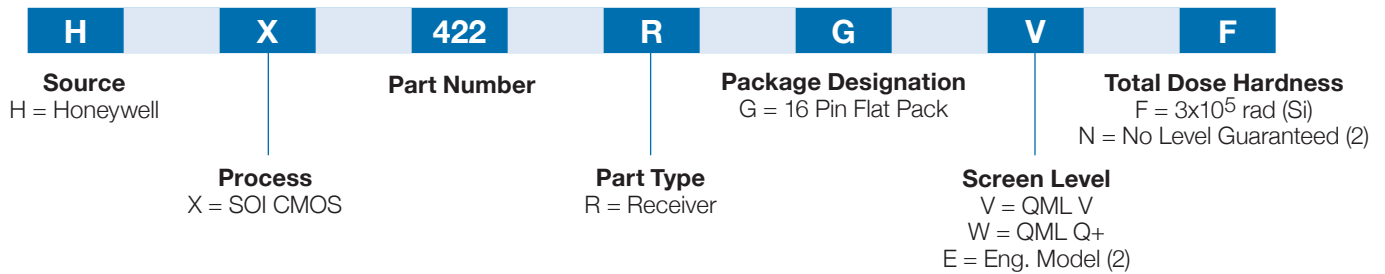
Conformance Summary

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

Ordering Information

Standard Microcircuit Drawing

The HX422R can be ordered under the SMD drawing 5962-07A04.



(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 for further information.

(2) Engineering Device Description: Engineering Model suffix for Screening Level and Total Dose hardness shall be "EN".

Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation hardness guaranteed.

QCI Testing (1)

Classification	QCI Testing
QML Q+	No lot specific testing performed. (2)
QML V	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell Quality Management Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.

(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

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Find out more

To learn more about Honeywell's radiation hardened integrated circuit products and technologies, visit www.honeywellmicroelectronics.com/

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