Radiation Hardened SOI CMOS Technology

Honeywell has been at the forefront of radiation hardened integrated circuit (IC) technologies for decades. The radiation hardened electronics are built upon a foundation of Silicon on Insulator Complementary metal–oxide–semiconductor (SOI CMOS) technology which is ideal for both digital and mixed signal space microelectronics.

SOI CMOS Technology Features and Benefits

The SOI CMOS technology is a key factor in providing excellent performance of the IC in radiation prone environments. Performance and reliability are significantly increased by incorporating a silicon dioxide layer to isolate the transistors from the substrate. General performance of SOI CMOS over Bulk CMOS is enhanced through:

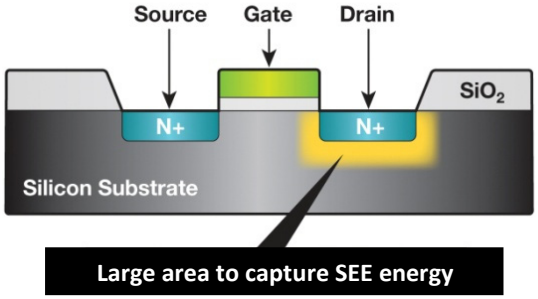
- **Reduce Parasitics** - Isolation from the bulk silicon substrate reduces capacitive loading which delivers high speed performance and lower power consumption.
- **Low Noise and Crosstalk** - SOI CMOS enables novel process and design techniques to achieve a very low noise operation and 4-6 dB lower cross-talk to support high performance mixed mode circuits. This is very beneficial for functions like SERDES, A/D Converters, PLLs, and low noise voltage references.

Radiation Performance of SOI CMOS based products

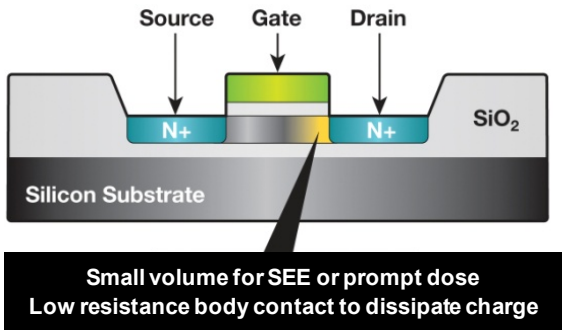
Our specialized, proprietary radiation hardened methods and techniques are used on multiple geometries (including 0.15µm, 0.35µm and 0.8µm) and at all levels of the product development to deliver radiation hardness with unmatched efficiency.

Charge Collection Volume – The isolation of the transistor from the bulk silicon substrate greatly reduces the charge collection volume within the integrated circuit. By reducing the volume to capture energy, the sensitivity to radiation, for single event and prompt dose environments, is greatly reduced. Charge collection volume shown in yellow.

Bulk CMOS



Honeywell SOI CMOS



Additional techniques and methodologies are applied throughout the development process in order to improve the radiation performance. These levels include:

- Wafer process and transistor design
- Modeling
- Circuit design
- Layout
- Package

Many circuit designs and layout hardening techniques are embedded in the library of hardened circuit elements. Your designs are synthesized using the hardened libraries, which reduces the dependence on redundant circuitry, which reduces chip area, lowers power and increases the performance of the product.

The SOI CMOS technology and design features will enable operation in the following typical radiation environments.

Parameter	Capabilities (1)
Total Ionizing Dose	**1 Mrad(Si)**
Single-Event-Upset (2)	**< 1E-11 e/b-d**
Single-Event-Latchup	**Immune**
Neutron Irradiation	**1E14 MeV eq. n/cm^2**
Dose-Rate Upset	**1E10 rad(Si)/s**
Dose-Rate Survivability	**1E12 rad(Si)/s**

Note:

(1) There is some variance between products. See datasheets for detailed specifications.

(2) Geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield.

No Latchup - SOI inherently eliminates latchup, which can occur in CMOS devices due to a parasitic condition in which at least one PNP and at least one NPN transistor act like a silicon controlled rectifier (SCR). This parasitic PNP structure creates a low-impedance path between the power rails and can permanently damage the device.

Find out more

For additional general information on Microelectronics, please visit aerospace.honeywell.com/microelectronics. For more technical inquiries about Honeywell's Microelectronics, please contact us at MicroelectronicsTechnicalInquiries@honeywell.com.

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